



iT2325A

Half Bridge Driver

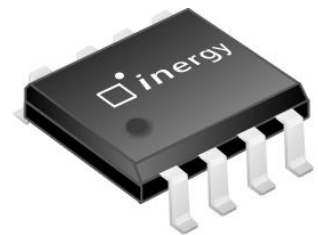
Preliminary Datasheet Rev. 0.1

1. Description

The iT2325A is a high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized construction. The logic input is compatible with standard CMOS or LSTTL output. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 650 volts.

2. Features

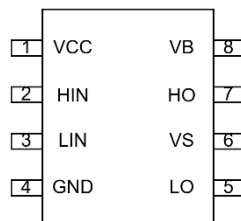
- Floating channel designed for bootstrap operation to + 650 V
- Gate driver supply range from 10 to 18 V
- Under-voltage lockout
- 3.3 V and 5 V logic compatible
- Driver source/sink peak current up to 0.3A/0.6A
- Internal minimum set dead-time
- High side output in phase with HIN



3. Applications

- BLDC motor driver
- E-bike
- Class D power audio amplifier


4. Pin Assignments



SOP-8L

Fig.1 Pin Assignments (Top View)

5. Marking Information

Product Name	Marking
iT2325A	 <p>X: Date code</p>

6. Ordering Code

Ordering Code
iT2325A

7. Pin Definitions

Pin No.	Symbol	Description
1	VCC	Low side and logic fixed power supply
2	HIN	Logic input for high side gate driver output, in phase with HO
3	LIN	Logic input for low side gate driver output, in phase with LO
4	GND	Ground terminal
5	LO	Low side gate driver output
6	VS	High side floating power supply return
7	HO	High side gate driver output
8	VB	High side floating power supply

8. Function Block

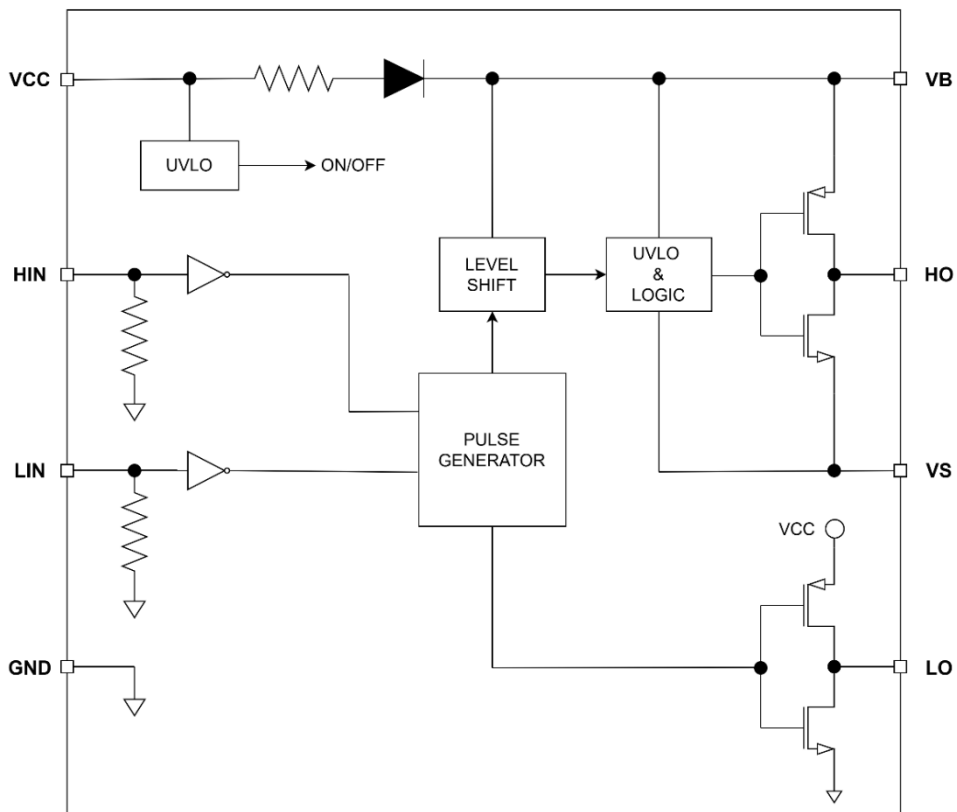


Fig.2 Pin Configuration and Internal Block Diagram

9. Typical Application Circuit

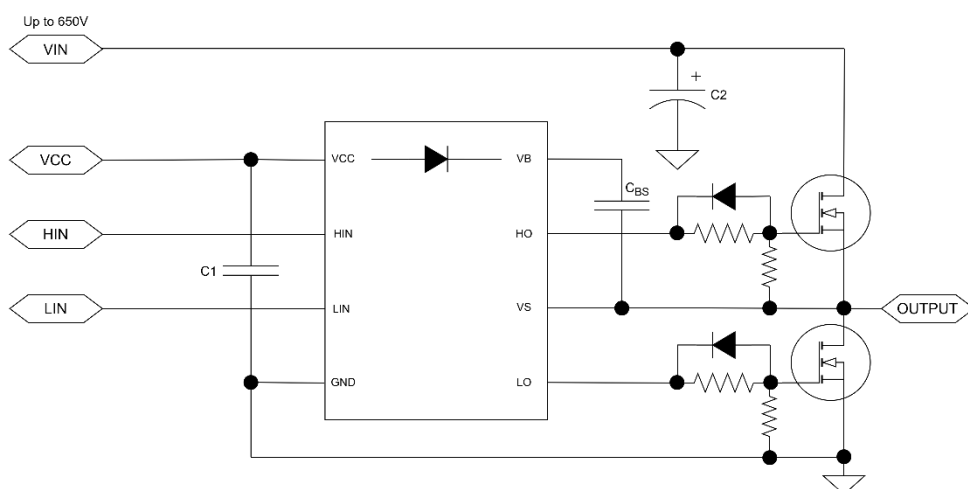


Fig.3 Application Circuit

Note 1 : Suggest that the $C_{BS} > 1.0\mu\text{F}$ and the $C1 > 10 \cdot C_{BS}$ (10 μF).

Note 2 : C1 & C_{BS} are placed close to the iT2325A's pins.

10. Electrical Characteristics

10.1 Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. The ambient temperature is 25°C.

Symbol	Parameter	MIN	MAX	Unit
V _B	High side floating supply voltage	- 0.3	670	V
V _S	High side floating supply offset voltage	-0.3	650	
V _{HO}	High side floating output voltage	V _S - 0.3	V _B + 0.3	
V _{CC}	Low side and logic fixed supply voltage	- 0.3	20	
V _{LO}	Low side output voltage	- 0.3	V _{CC} + 0.3	
V _{IN}	Logic input voltage	- 0.3	V _{CC} + 0.3	
P _D	Package power dissipation @ T _A ≤ + 25 °C	—	0.625	W
R _{thJA}	Thermal resistance, junction to ambient	—	200	°C / W
T _J	Junction temperature	-40	150	°C
T _S	Storage temperature	- 55	150	
T _L	Lead temperature (soldering, 10 seconds)	—	300	

10.2 Recommended Operating Conditions

For proper operation, the devices should be used under the following recommended conditions.

Symbol	Parameter	MIN	MAX	Unit
V _B	High side floating supply absolute voltage		V _S + 18	V
V _S	High side floating supply offset voltage	- 0.3	600	
V _{HO}	High side floating output voltage	V _S	V _B	
V _{CC}	Low side and logic fixed supply voltage	10	18	
V _{LO}	Low side output voltage	0	V _{CC}	
V _{IN}	Logic input voltage	0	V _{CC} +0.3	
T _A	Ambient temperature	- 40	125	°C

10.3 D.C. and A.C. Characteristics

10.3.1 DC Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 15\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$ unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to GND. The V_O and I_O parameters are referenced to GND and are applicable to the respective output leads: HO or LO.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{IH}	Logic " 1 " input voltage	$V_{CC} = 10\text{ V to }15\text{ V}$	2.0			V
V_{IL}	Logic " 0 " input voltage	$V_{CC} = 10\text{ V to }15\text{ V}$			1.2	
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	$I_O = 20\text{ mA}$		0.5		V
V_{OL}	Low level output voltage	$I_O = 20\text{ mA}$		0.25		
I_{LK}	Offset supply leakage current	$V_B = V_S = 600\text{ V}$			10	uA
I_{QBS}	Quiescent V_{BS} supply current	$V_{IN} = 0\text{ V}$		20		
I_{QCC}	Quiescent V_{CC} supply current	$V_{IN} = 0\text{ V}$		50		
I_{IN+}	Logic " 1 " input bias current	$V_{IN} = 5\text{ V}$	1.7		70	
I_{IN-}	Logic " 0 " input bias current	$V_{IN} = 0\text{ V}$	-5		5	
V_{CCUV+}	V_{CC} supply under voltage positive going threshold		8.0	8.9	9.8	V
V_{CCUV-}	V_{CC} supply under voltage negative going		7.5	8.4	9.3	V
V_{BSUV+}	V_{BS} supply under voltage positive going threshold		7.2	8.2	9.2	V
V_{BSUV-}	V_{BS} supply under voltage negative going		6.4	7.3	8.3	V
R_{IN}	HIN, LIN pin pull low resistor			100		K Ω
I_{O+}	Peak output current turn-on	$V_O=0V, PW \leq 10\mu s$		300		mA
I_{O-}	Peak output current turn-off	$V_O=15V, PW \leq 10\mu s$		600		mA
R_{BS}	Boot strap diode series resistor			310		Ω

10.3.2 AC Characteristics

$V_S=310V$, $V_{CC}=15V$, $V_{SS} = GND$, $C_L = 1nF$, $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified.

Symbol	Definition	Test Conditions	MIN	TYP	MAX	Units
t_{on}	Turn-on propagation delay			175		ns
t_{off}	Turn-off propagation delay			185		
$t_{PW\ min}$	HIN, LIN minimum pulse width			70		
t_r	Turn on rise time (10%~90%)	$C_L = 1\text{ nF}$		50		
t_f	Turn off fall time (90%~10%)	$C_L = 1\text{ nF}$		50		
PM	Output pulse width matching ($ PW_{IN} - PW_{OUT} $)	Pulse width > 1us			100	ns
MT	Delay matching time (HS & LS turn-on/off)	External dead time > 800ns			50	ns
t_{DT}	Short through prevention dead time		300	500	700	ns

10.3.3 Truth Table

HIN	LIN	HO	LO
0	0	0	0
0	1	0	1
1	0	1	0
1	1	0	0

10.3.4 The switching time definition are shown in the figures below

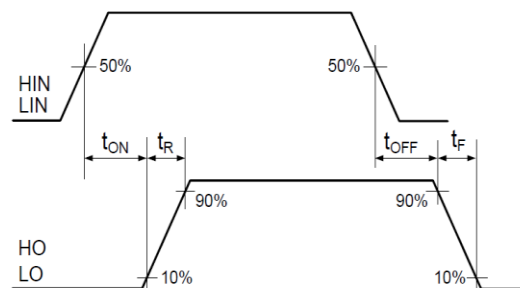


Fig.4 Switching Time Definitions

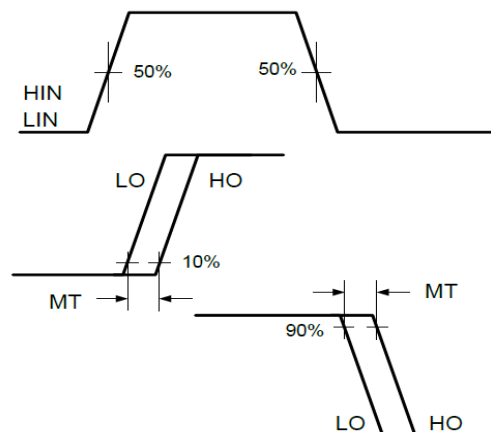


Fig.5 Delay Matching Waveform Definition

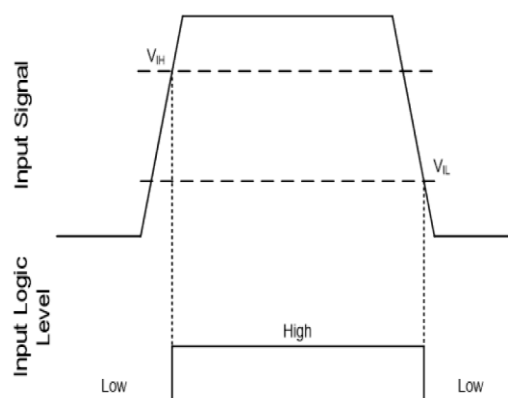
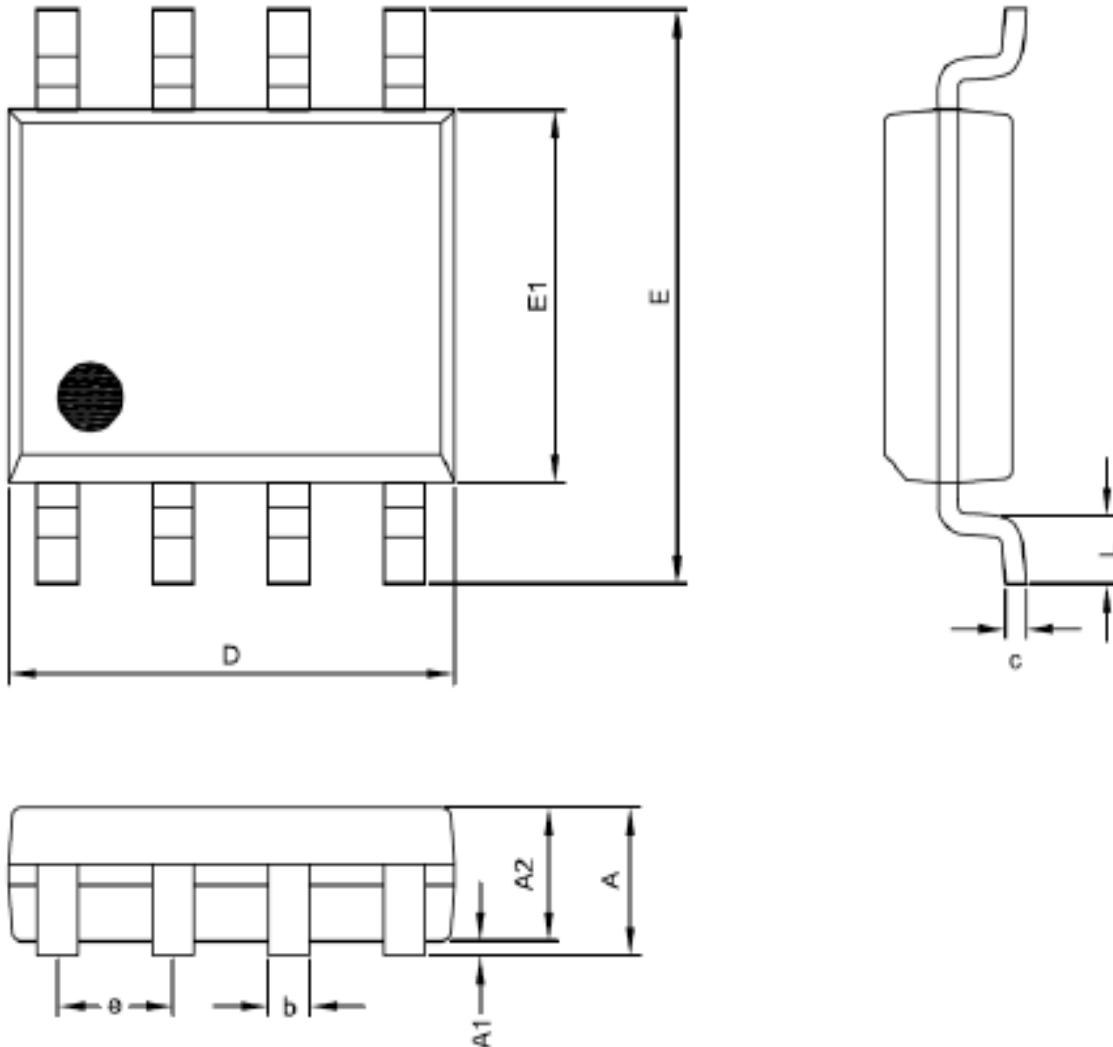


Fig.6 HIN & LIN Input Thresholds

11. Package Information

SOP-8L Outline Dimensions



Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	1.35	1.75
A1	0.00	0.25
A2	1.15	1.50
D	4.80	5.00
E	5.80	6.20
E1	3.80	4.00
c	0.19	0.27
b	0.33	0.53
e	1.27 BSC	
L	0.40	1.27

Notes :

1. Jedec outline : MS-012AA
2. Dimensions " D " does not include mold flash, protrusions and gate burrs shall not exceed .15 mm (.006 in) per side .
3. Dimensions " E1 " does not include inter-lead flash, or protrusions. Inter-lead flash and protrusions shall not exceed .25 mm (.010 in) per side.

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