

1. Description

The iU6291 is a single-phase BLDC motor controller IC integrated with various peripherals to realize BLDC motors application. The logic input is compatible with standard CMOS output. It features the flexibility to adjust various motor parameters and complete protection such as over current, over voltage and under voltage lockout. Moreover, its operation current is only ~10mA and a low power stop mode can further save the power when the motor stops rotating.

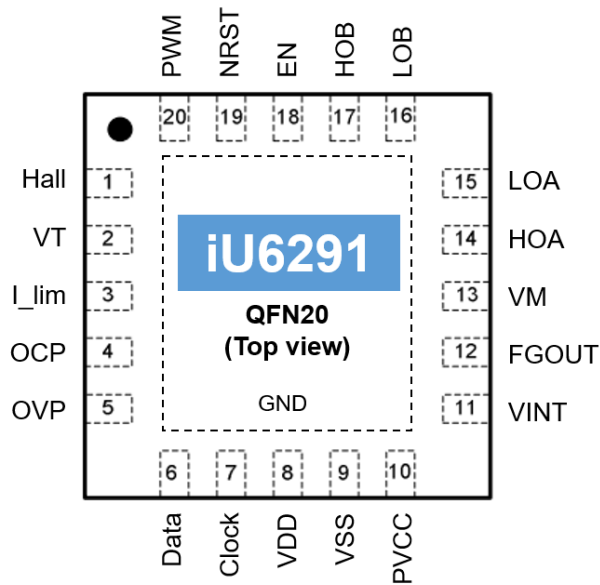
2. Features

- Single-Phase BLDC Motor Controller
- Operating Supply Voltage from 7V to 32V
- Embedded P/N MOS Pre-driver
- FG Open Drain MOSFET
- Programmable Locked Rotor and Restart Timing
- Programmable Soft Start Timing
- Complete Protection OCP/OVP/UVLO
- QFN-20 4x4 Package


3. Applications

- BLDC Motor Driver

4. Pin Assignments



5. Marking Information

Product Name	Marking
iU6291	 <p>X: Date code</p>

6. Ordering Code

Ordering Code
iU6291

7. Pin Definitions

Pin No.	Symbol	Description
1	Hall	Hall Input
2	VT	PWM Input Threshold
3	I_lim	Average Current Detection
4	OCP	Over Current Protection
5	OVP	Over Voltage Protection
6	Data	Data Input
7	Clock	Clock Input
8	VDD	Self Logic 5V Power
9	VSS	Ground
10	PVCC	Power VCC Supply
11	VINT	7V Regulator Output for Pre-Driver
12	FGOUT	FG Output
13	VM	VDC Supply, HO Pull-Hi Voltage
14	HOA	A-Phase, High Side Gate Driver
15	LOA	A-Phase, Low Side Gate Driver
16	LOB	B-Phase, Low Side Gate Driver
17	HOB	B-Phase, High Side Gate Driver
18	EN	Pre-Driver Enable
19	NRST	External RESET
20	PWM	PWM Input

8. Electrical Characteristics

8.1 Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Parameter	Min.	Max.	Unit
V _{HO}	High Side Floating Output Voltage	VM - 7	VM + 0.3	V
PVCC	Low Side Power Supply Voltage	- 0.3	40	V
VM	High Side Power Supply Voltage	- 0.3	40	V
I/O Pin	Logic Input Voltage	- 0.3	VDD + 0.3	V
T _J	Junction Temperature	-	125	°C
T _S	Storage Temperature	-55	150	

8.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
PVCC	Low Side Power Supply Voltage	7	32	V
I/O Pin	Logic Input Voltage	0	VDD + 0.3	V
T _A	Ambient Temperature (*Note)	- 40	105	°C

*Note : Please do not exceed T_J limitation

8.3 D.C. Characteristics

Symbol	Conditions			Min.	Typ.	Max	Unit
	Mode	f _{HCLK}	Conditions				
IDD	Operation Mode Internal Clock	60MHz	All Peripherals Enabled	-	8.61	-	mA
			All Peripherals Disabled	-	7.08	-	mA
		40KHz	All Peripherals Enabled	-	1.02	-	mA
			All Peripherals Disabled	-	1.00	-	mA
	Sleep Mode, Internal Clock	60MHz	All Peripherals Enabled	-	3.52	-	mA
			All Peripherals Disabled	-	2.25	-	mA
		40KHz	All Peripherals Enabled	-	1.00	-	mA
			All Peripherals Disabled	-	1.00	-	mA
	Stop Mode	-	Enter Stop Mode after Reset	-	110	-	uA

8.4 A.C. Characteristics

8.4.1 High Speed Internal Oscillator (HSI) Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
f_{HSI}	Frequency	-	-	60	-	MHz
ACC_{HSI}	Accuracy of HSI Oscillator	$T_A = -40^{\circ}C \sim 105^{\circ}C$	-2.5	-	+2.5	%
		$T_A = -10^{\circ}C \sim 85^{\circ}C$	-1.5	-	+1.5	%
		$T_A = 25^{\circ}C$	-1	-	+1	%

8.4.2 Low Speed Internal Oscillator (LSI) Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
F_{LSI}	Frequency	$T_A = -40^{\circ}C \sim 105^{\circ}C$	20	40	60	KHz
$tsu_{(LSI)}$	LSI Oscillator Start-up Time	-	-	-	300	us
$IDD_{(LSI)}$	Power Consumption of LSI Oscillator	-	-	0.34	-	uA

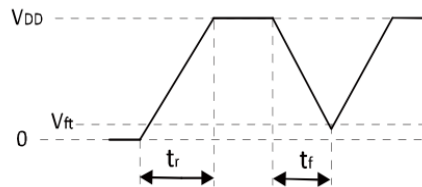
8.4.3 Power-up and Power-down Characteristics

Symbol	Conditions	Min.	Typ.	Max	Unit
t_{VDD}	VDD Rising Time t_r	300	-	50000	us
	VDD Falling Time t_f	300	-	50000	
V_{ft}	Power-down Threshold Voltage	0	-	-	mV

Note 1 : Derived from overall evaluation, not tested in production.

Note 2 : The on-chip VDD waveform during power-down should follow the t_r and t_f stages as shown in the waveform diagram below.

Note 3 : The chip should be powered up from 0V to ensure reliable power-up.



8.4.4 Low-Power Mode Wake-up Time

Symbol	Conditions	Min.	Typ.	Max	Unit
$t_{WUSLEEP}$	Wake-up from Sleep Mode (System Clock is HSI)	-	1.5	-	us
t_{WUSTOP}	Wake-up from Stop Mode (System Clock is HSI)	-	65	-	us

8.5 Input / Output Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
V _{IL}	Input low-level voltage	5V CMOS port	-	-	0.3 * VDD	V
V _{IH}	Input high-level voltage	5V CMOS port	0.7 * VDD	-	-	V
V _{hy}	I/O pin Schmitt trigger voltage hysteresis	5V	0.1 * VDD	0.60	-	V
I _{lkg}	Input leakage current	5V	-1	-	1	μA
R _{PU}	Weak pull-up equivalent resistor	5V VIN = VSS	50	60	75	kΩ
R _{PD}	Weak pull-down equivalent resistor	5V VIN = VSS	50	60	75	kΩ
C _{IO}	I/O pin capacitance	-	-	-	10	pF

Symbol	Parameter	Conditions	Typ.	Unit
V _{OL}	Output low level	I _{IO} = 6mA , VDD = 5V	0.11	V
V _{OH}	Output high level		4.83	
V _{OL}	Output low level	I _{IO} = 8mA , VDD = 5V	0.15	
V _{OH}	Output high level		4.78	
V _{OL}	Output low level	I _{IO} = 20mA , VDD = 5V	0.38	
V _{OH}	Output high level		4.4	

8.6 POR / PVD Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
V _{VPD}	Level Selection for Programmable Voltage Detector	Rising Edge: Level 1	-	2.4	-	V
		Falling Edge: Level 1	-	2.3	-	V
		Rising Edge: Level 2	-	2.7	-	V
		Falling Edge: Level 2	-	2.6	-	V
		Rising Edge: Level 3	-	3.0	-	V
		Falling Edge: Level 3	-	2.9	-	V
		Rising Edge: Level 4	-	3.3	-	V
		Falling Edge: Level 4	-	3.2	-	V
		Rising Edge: Level 5	-	3.6	-	V
		Falling Edge: Level 5	-	3.5	-	V
		Rising Edge: Level 6	-	3.9	-	V
		Falling Edge: Level 6	-	3.8	-	V
		Rising Edge: Level 7	-	4.2	-	V
		Falling Edge: Level 7	-	4.1	-	V
		Rising Edge: Level 8	-	4.5	-	V
		Falling Edge: Level 8	-	4.4	-	V
		Rising Edge: Level 9	-	4.8	-	V
		Falling Edge: Level 9	-	4.7	-	V
V _{POR}	Power-on Reset Threshold	-	-	2.2	-	V
V _{hyst_POR/PDR}	POR/PDR Hysteresis	-	-	60	-	mV
T _{RSTTEMPO}	Reset Duration	-	-	1.84	-	ms

8.7 A/D Converter Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
V _{DD}	Supply Voltage	-	2.5	-	5.5	V
f _{ADC}	ADC Clock Frequency	V _{DD} ≥ 2.5V	-	-	15	MHz
f _s	Sampling Rate	12bits; V _{DD} ≥ 2.5V	-	-	1	MHz
f _{TRIG}	External trigger frequency	12bits; f _{ADC} = 15MHz	-	-	1	MHz
		12bits	-	-	15	1/ f _{ADC}
R _{AIN}	External Input Impedance	-	See the formula below			KΩ
R _{ADC}	Sampling switch resistance	-	-	-	1.5	KΩ
C _{ADC}	Internal sampling and holding capacitance	-	-	-	5	pF
t _{STAB}	Power-up Time	-	-	-	10	μS
t _{lat}	Injection-Trigger Conversion Delay	-	-	-	512	1/f _{ADC}
t _{latr}	Regular-Trigger Conversion Delay	-	-	-	512	1/f _{ADC}
t _s	Sampling Time	f _{ADC} = 15MHz	0.167	-	16.03	μS
t _{CONV}	Total Conversion Time (including Sampling Time)	12bits; f _{ADC} =15MHz	1	-	16.87	μS
ENOB	Effective Number of Bits	12bits; V _{DD} ≥ 3.3V; f _{ADC} = 15MHz	-	10.9	-	bit

Note: For external triggering, a delay of 1/f_{ADC} must be added to the timing

Input Impedance Table

$$R_{AIN} < \frac{T_s}{f_{ADC} \times C_{ADC} \times \ln(2^{n+2})} - R_{ADC}$$

The above formula is used to determine the maximum external impedance to ensure that the error is less than 1/4 LSB. Here, n = 12 (representing 12-bit resolution) and it is measured at f_{ADC} = 15MHz.

Symbol	Parameter	Conditions	Typ.	Unit
ET	Overall Error	f _{PCLK1} =60MHz, f _{ADC} =15MHz, R _{AIN} <0.1KΩ, V _{DD} =5V, T _A =25°C	-4.7 to +3.4	LSB
EO	Offset Error		-1.9 to +2.8	LSB
EG	Gain Error		-0.4 to +1.6	LSB
ED	Differential Linearity Error		-1.0 to +0.4	LSB
EL	Integral Linearity Error		-2.2 to +3.4	LSB

8.8 Comparator Electrical Characteristics

Symbol	Parameter	Register Configuration	Min.	Typ.	Max	Unit
t _{HYST}	Hysteresis	00(hysteresis), high power	-	0	-	mV
		00(hysteresis), low power	-	0	-	mV
		01(hysteresis), high power	15	22	43	mV
		01(hysteresis), low power	13	15	23	mV
		10(hysteresis), high power	32	45	92	mV
		10(hysteresis), low power	25.2	32	46.7	mV
		11(hysteresis), high power	55	85	182	mV
		11(hysteresis), low power	25.5	60	83.9	mV
V _{OFFSET}	Offset Voltage	-		+/-6	+/-10.4	mV
t _{DELAY}	Propagation Delay ^{Note1}	00 (high power)	3.7	10.7	43	ns
		01 (medium power)	10.5	34.9	83	ns
		10 (low power)	13.8	49	114	ns
		11 (ultra-low power)	22.2	86	194.5	ns
I _q	Average Operating Current	00 (high power)	6.5	45	205.4	μA
		01 (medium power)	3.3	21.7	81.3	μA
		10 (low power)	2.6	15.3	59.6	μA
		11 (ultra-low power)	1.7	8.8	35.3	μA

Note1 : Time difference between 50% output transistor and input transition.

8.9 P/N MOSFET Gate-driver with LDO Electrical Characteristics

8.9.1 Driver Section

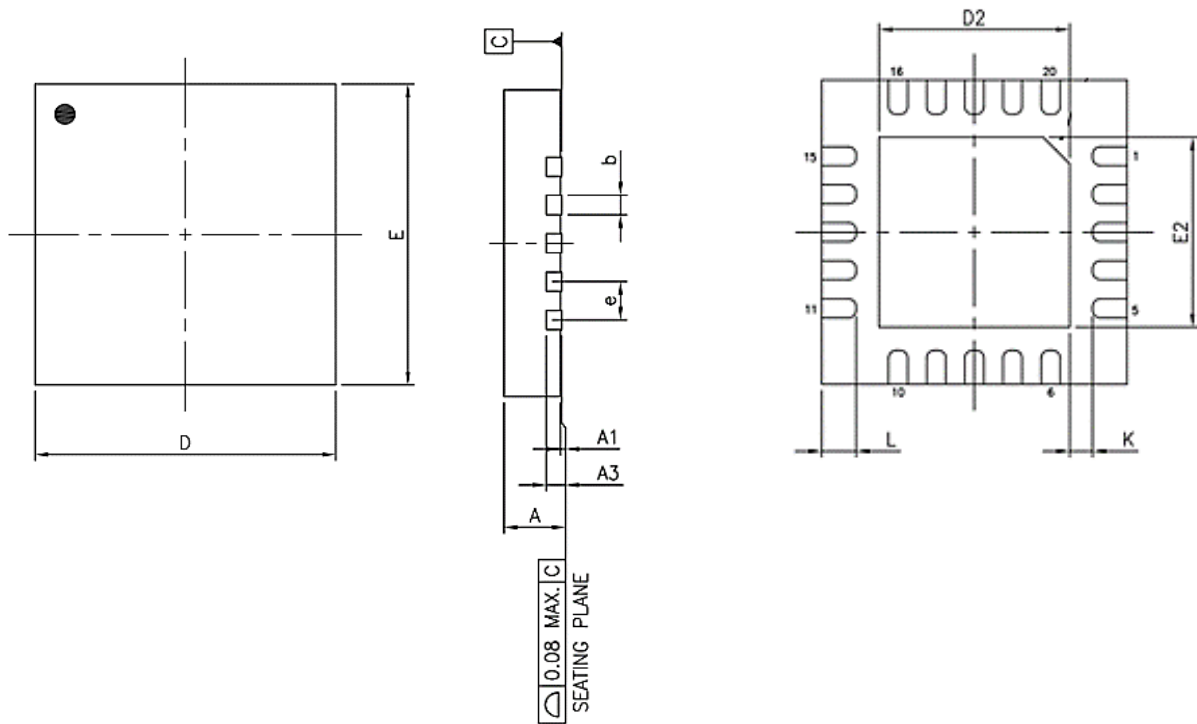
Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
V _{H_{SOH}}	Hi-side PMOS off, VM - VHO	I _o = 2mA	-	0.24	-	V
V _{L_{SOH}}	Low-side NMOS off	I _o = 2mA	-	V _{INT} - 0.2	-	V
I _{HOL}	High-Side turn-on current	-	-	35	-	mA
I _{LOH}	Low-Side turn-on current	-	-	45	-	mA
I _{op}	Operating current	-	-	-	30	mA
V _{CCUV+}	PVCC supply under voltage positive going threshold	-	6.2	6.6	7	V
V _{CCUV-}	PVCC supply under voltage negative going threshold	-	5.9	6.3	6.7	V
V _{HOCLP}	HO clamp, VM - VHO	-	6.5	7	7.5	V

8.9.2 LDO Section

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
V _{INT}	Internal regulator output voltage	I _{VINT} = 5 mA	6.5	7	7.5	V
I _{VINT}	VINT output current	V _{INT} = 6.5 V	10	-	-	mA
V _{DD}	5V regulator output voltage	I _{VDD} = 10 mA	- 5%	5	+ 5%	V
I _{VDDMAX}	VDD max output current	V _{DD} = 4.5 V	-	-	20	mA

9. Package Information

QFN-20 (4.0 x4.0 mm) Outline Dimensions



SYMBOL	Dimension in mm		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.20	0.25	0.30
D	4.00 BSC		
E	4.00 BSC		
e	0.50 BSC		
D2	2.45	2.60	2.75
E2	2.45	2.60	2.75
K	0.20	-	-
L	0.35	0.45	0.55

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