iMN2R0N08G

N-Channel Enhancement Mode MOSFET

Datasheet

1. Product Information

1.1 Features

- Surface-mount Package
- Advanced Trench Technology
- RoHS Compliant and Halogen Free
- Reliable and Rugged
- Key Applications：Motor Drivers, DC-DC Converter



1.2 Package Type

PDFN5X6B-EP1-8L

1.3 Quick Reference

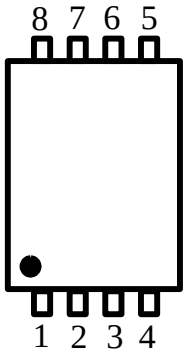
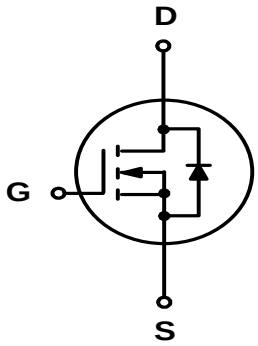
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Limiting Values						
P_{tot}	Total Power Dissipation	T_C = 25 ℃	-	-	300	W
I_{DS} Note1	Drain-Source Current	T_C = 25 ℃, V_{GS} = 10 V	-	-	100	A
		T_C = 100 ℃, V_{GS} = 10 V	-	-	100	
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	80	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250 μA	2	-	4	
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS} = 10 V, I_D = 60 A	-	2.1	2.6	mΩ
		V_{GS} = 6 V, I_D = 30 A	-	2.9	3.8	

2. Ordering Code & Marking Information

Ordering Code	Marking Information
iMN2R0N08G	2R0N08 XXXXXX X：Date Code

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3. Pin Description

Pin	Description	Simplified Outline	Symbol
1,2,3	Source(S)		
4	Gate(G)		
5,6,7,8	Drain(D)		

4. Limiting Values

Symbol	Parameter		Rating	Unit
V_{DS}	Drain-Source Voltage		80	V
V_{GS}	Gate-Source Voltage		± 20	
I_{DS} Note1	Drain-Source Current	T_C = 25 ℃, V_{GS} = 10 V	100	A
		T_C = 100 ℃, V_{GS} = 10 V	100	
I_{DM} Note1,2	Pulsed Drain-Source Current	T_C = 25 ℃, V_{GS} = 10 V	400	A
I_S Note1	Diode Forward Current	T_C = 25 ℃, V_{GS} = 0 V	100	A
E_{AS}	Single Pulsed Avalanche Energy	V_{DD} = 50 V, L = 1 mH	220	mJ
P_{tot}	Total Power Dissipation	T_C = 25 ℃	300	W
$R_{\theta JA}$ Note3	Thermal Resistance- Junction to Ambient		55	℃ / W
$R_{\theta JC}$	Thermal Resistance- Junction to Case		0.5	
T_{stg}	Storage Temperature		- 55 ~ 175	℃
T_J	Junction Temperature		175	℃

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5. Electrical Characteristics (T_A = 25 °C Unless Otherwise Noted)

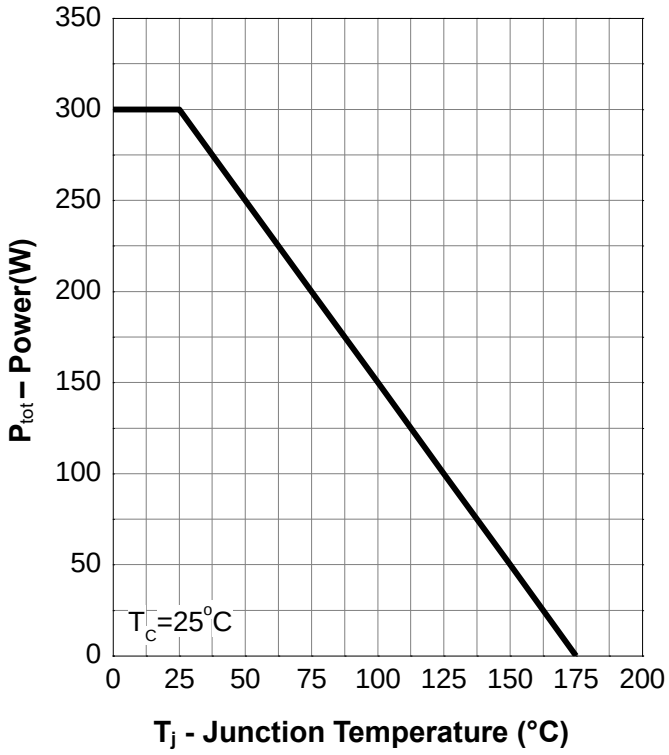
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	80	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250 μA	2	-	4	
I_{DSS}	Drain Leakage Current	V_{DS} = 64 V, V_{GS} = 0 V	-	-	1	μA
I_{GSS}	Gate Leakage Current	V_{GS} = ± 20 V, V_{DS} = 0 V	-	-	± 100	nA
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS} = 10 V, I_D = 60 A	-	2.1	2.6	mΩ
		V_{GS} = 6 V, I_D = 30 A	-	2.9	3.8	
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_{SD} = 60 A, V_{GS} = 0 V	-	-	1.3	V
t_{rr} Note4	Reverse Recovery Time	I_{DS} = 60 A, dI_{SD}/dt = 100 A/μs	-	40	-	nS
Q_{rr} Note4	Reverse Recovery Charge		-	38	-	nC
Dynamic Characteristics Note4						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 40 V Frequency = 1 MHz	-	5531	-	pF
C_{oss}	Output Capacitance		-	845	-	
C_{rss}	Reverse Transfer Capacitance		-	62	-	
$R_{g(int)}$	Internal Gate Resistance	V_{GS} = 0 V, V_{DS} = 0 V, f = 1 MHz	-	1.1	-	Ω
$t_{d(on)}$	Turn-on Delay Time	V_{DS} = 40 V, V_{GEN} = 10 V, R_G = 3.9 Ω, R_L = 0.66 Ω, I_{DS} = 60 A	-	21	-	nS
t_r	Turn-on Rise Time		-	78	-	
$t_{d(off)}$	Turn-off Delay Time		-	63	-	
t_f	Turn-off Fall Time		-	53	-	
Gate Charge Characteristics Note4						
Q_g	Total Gate Charge	V_{GS} = 10 V, V_{DS} = 40 V, I_{DS} = 60 A	-	105	-	nC
Q_{gs}	Gate-Source Charge		-	31	-	
Q_{gd}	Gate-Drain Charge		-	28	-	

Note 1：Limitation by silicon chip.
Note 2：Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
Note 3：Surface Mounted on 1 in^2 pad area, t ≤ 10 sec.
Note 4：Guaranteed by design, not subject to production testing.

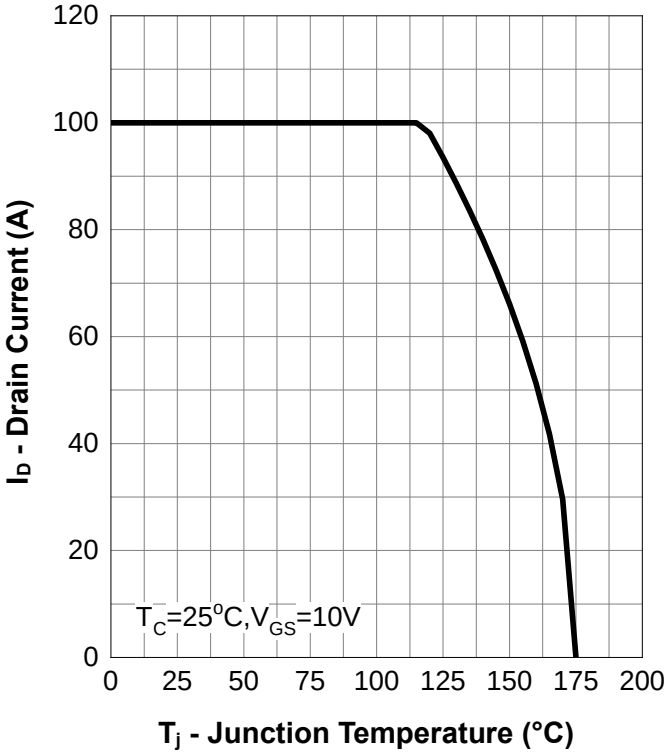
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6. Typical Characteristics

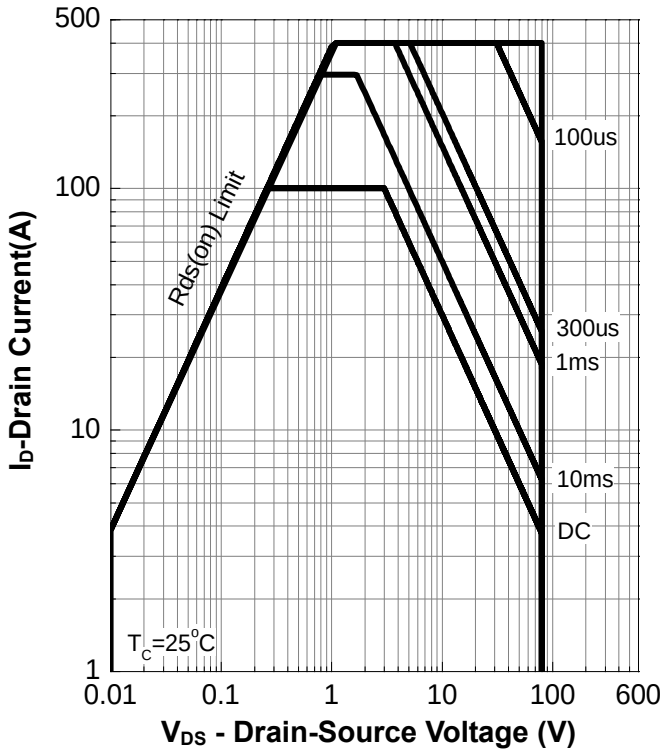
Power Capability



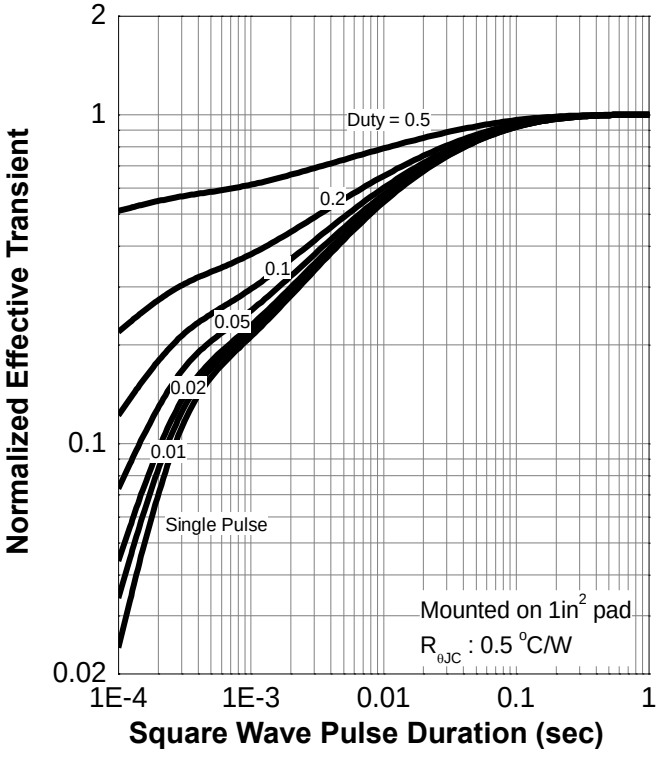
Current Capability



Safe Operation Area



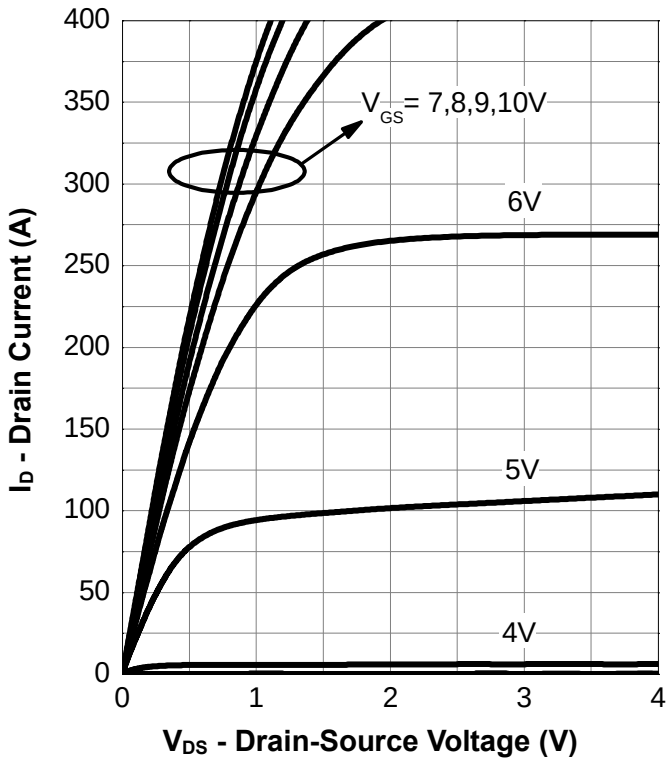
Transient Thermal Impedance



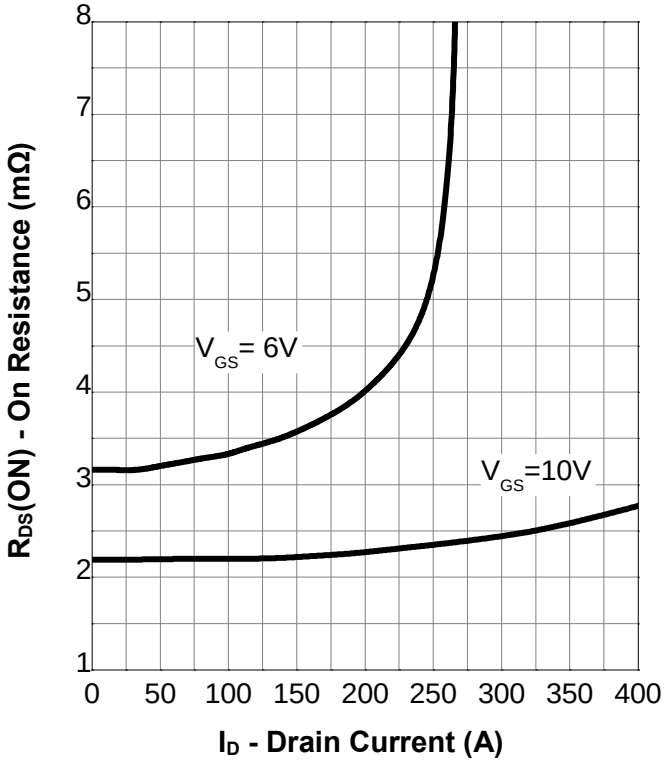
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6. Typical Characteristics (cont.)

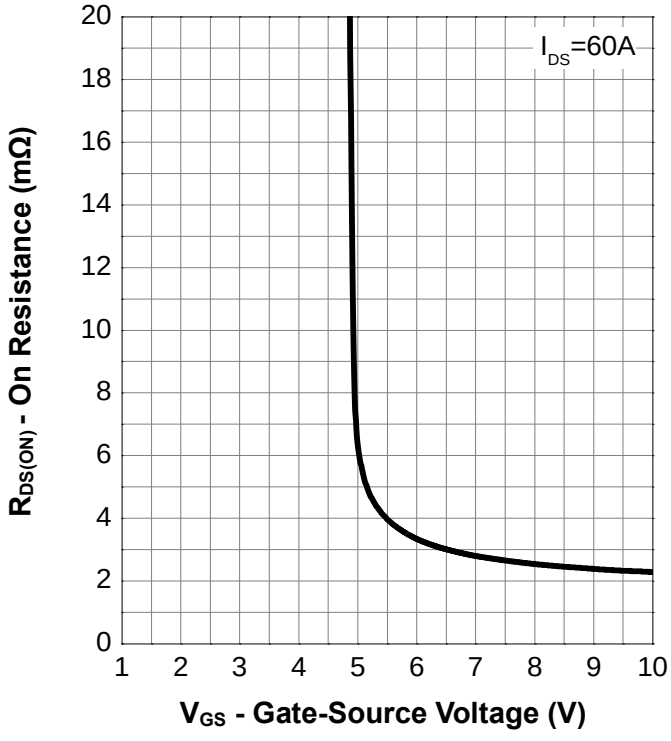
Output Characteristics



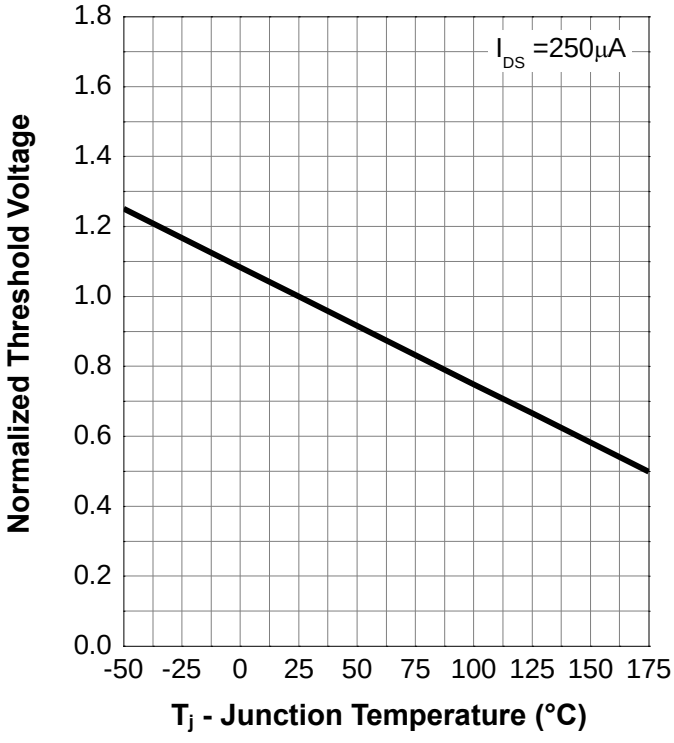
On Resistance



Transfer Characteristics



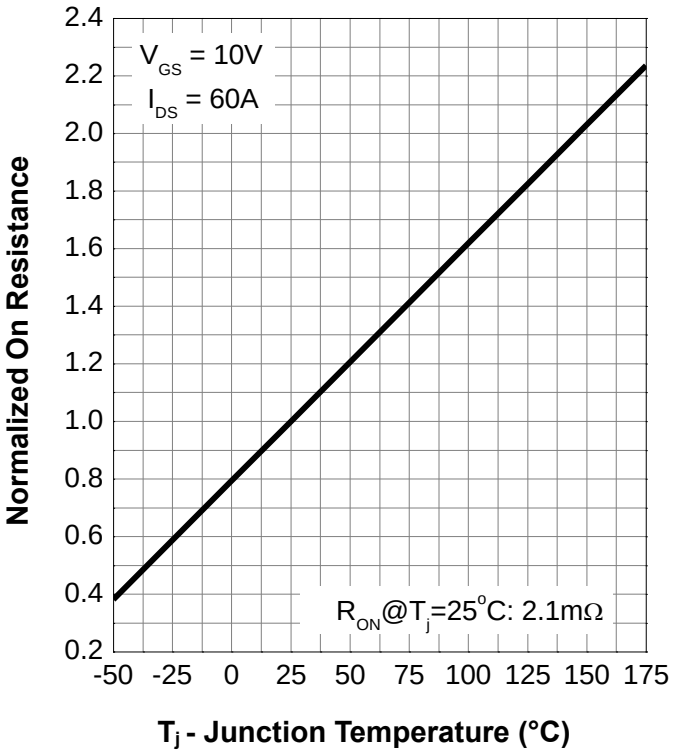
Normalized Threshold Voltage



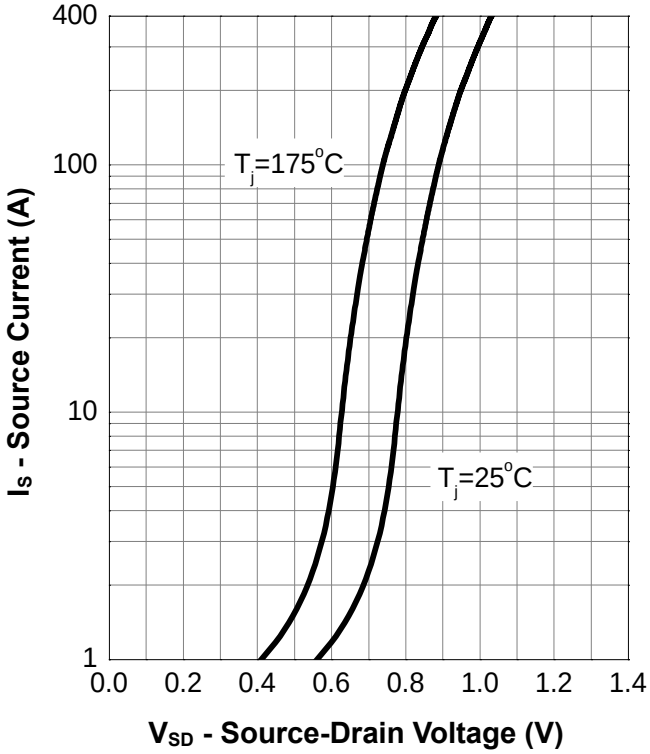
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6. Typical Characteristics (cont.)

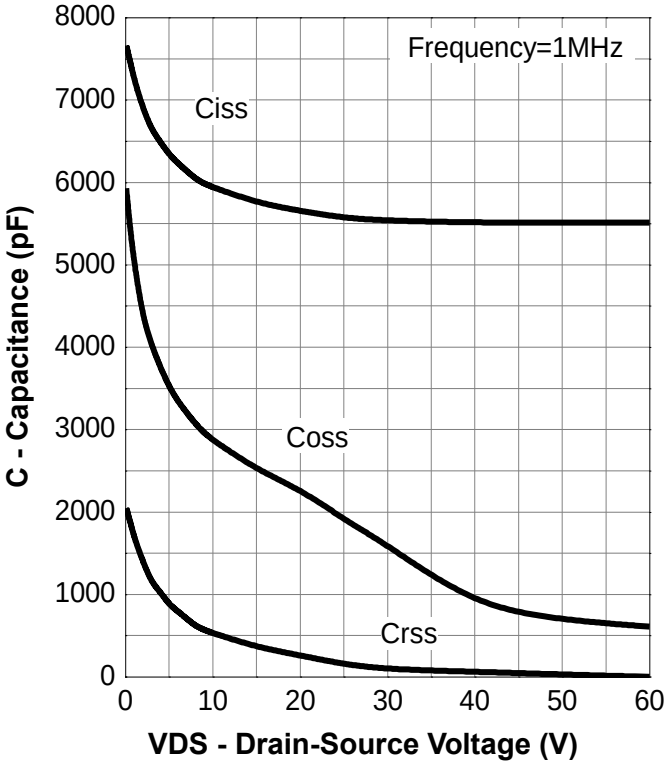
Normalized On Resistance



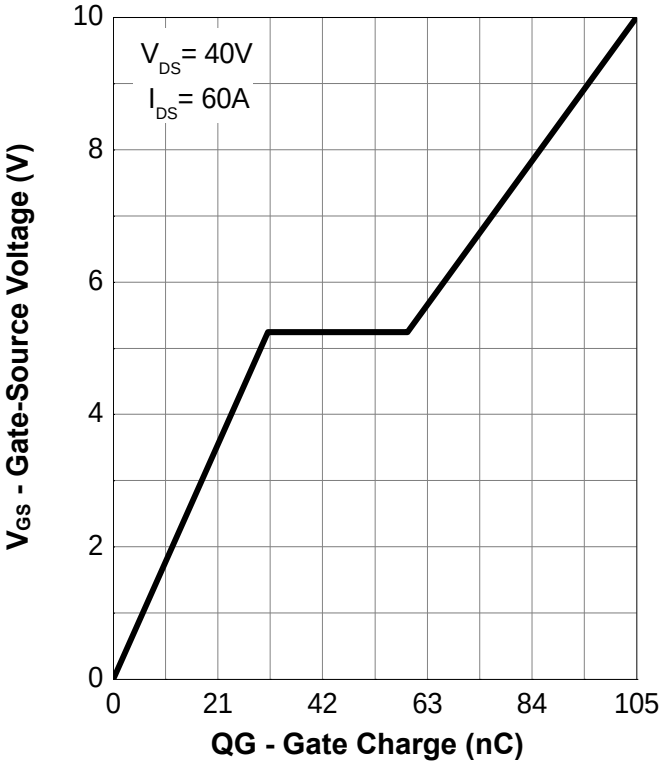
Diode Forward Current



Capacitance



Gate Charge



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