iMF409

N-Channel Enhancement Mode MOSFET

Datasheet

1. Product Information

1.1 Features

- Advanced Trench Cell Design
- RoHS Compliant and Halogen Free
- Reliable and Rugged
- Moisture Sensitivity Level MSL1



1.2 Package Type

LFPAK5X6-4L

1.3 Quick Reference

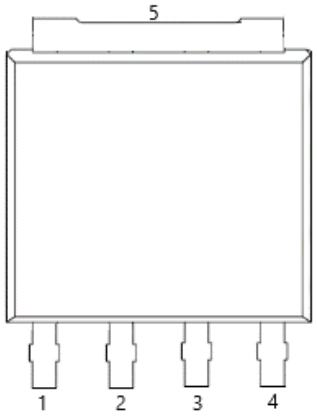
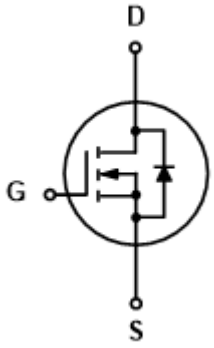
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Limiting Values						
P_{tot}	Total Power Dissipation	T_C = 25 ℃	-	-	333	W
I_{DS} Note1	Drain-Source Current	T_C = 25 ℃, V_{GS} = 10 V	-	-	300	A
		T_C = 100 ℃, V_{GS} = 10 V	-	-	300	
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 250 μA	30	-	-	V
$V_{GS(th)}$	Gate-Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250 μA	1	-	2	
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS} = 10 V, I_{DS} = 50 A	-	0.5	0.63	mΩ
		V_{GS} = 4.5 V, I_{DS} = 30 A	-	0.8	1.1	

2. Ordering Code & Marking Information

Ordering Code	Marking Information
iMF409	iMF409 XXXXX X: Date Code

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3. Pin Description

Pin	Description	Simplified Outline	Symbol
1~3	Source (S)		
4	Gate (G)		
5	Drain (D)		

4. Limiting Values

Symbol	Parameter		Rating	Unit
V_{DS}	Drain-Source Voltage		30	V
V_{GS}	Gate-Source Voltage		± 20	
I_{DS} Note1	Drain-Source Current	T_C = 25 ℃, V_{GS} = 10 V	300	A
		T_C = 100 ℃, V_{GS} = 10 V	300	
I_{DM} Note2	Pulsed Drain-Source Current	T_C = 25 ℃, V_{GS} = 10 V	1200	A
I_S	Diode Forward Current	T_C = 25 ℃, V_{GS} = 0 V	300	
E_{AS}	Single Pulsed Avalanche Energy	L = 1.0 mH, V_{DD} = 30 V	1922	mJ
P_{tot}	Total Power Dissipation	T_C = 25 ℃	333	W
$R_{\theta JA}$ Note3	Thermal Resistance- Junction to Ambient		56	℃ / W
$R_{\theta JC}$	Thermal Resistance- Junction to Case		0.45	
T_{stg}	Storage Temperature		- 55 ~ 175	℃
T_J	Junction Temperature		175	

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5. Electrical Characteristics (T_A = 25 °C Unless Otherwise Noted)

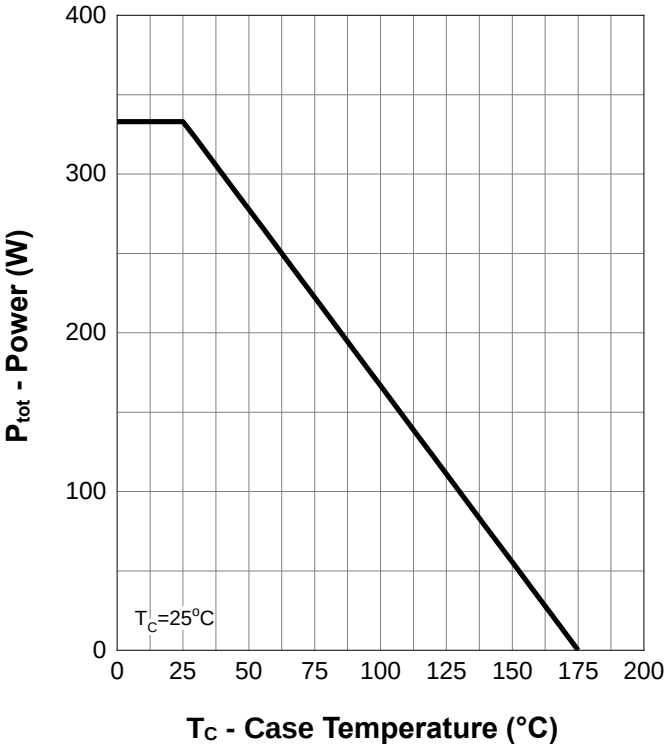
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 250 μA	30	-	-	V
$V_{GS(th)}$	Gate-Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250 μA	1	-	2	
I_{DSS}	Drain-Source Leakage Current	V_{DS} = 24 V, V_{GS} = 0 V	-	-	1	μA
I_{GSS}	Gate-Source Leakage Current	V_{DS} = 0 V, V_{GS} = ± 20 V	-	-	± 100	nA
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS} = 10 V, I_{DS} = 50 A	-	0.5	0.63	mΩ
		V_{GS} = 4.5 V, I_{DS} = 30 A	-	0.8	1.1	
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_{SD} = 50 A, V_{GS} = 0 V	-	-	1.3	V
t_{rr}[Note4]	Reverse Recovery Time	I_{DS} = 50 A, V_{GS} = 0 V dI_{SD}/dt = 100 A/μs	-	40	-	nS
Q_{rr}[Note4]	Reverse Recovery Charge		-	27	-	nC
Dynamic Characteristics[Note4]						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 15 V Freq. = 1 MHz	-	14707	-	pF
C_{oss}	Output Capacitance		-	1417	-	
C_{rss}	Reverse Transfer Capacitance		-	603	-	
$R_{g(int)}$	Internal Gate Resistance	V_{GS} = 0 V, V_{DS} = 0 V, Freq. = 1 MHz		1.3		Ω
t_d(on)	Turn-on Delay Time	V_{DS} = 15 V, V_{GEN} = 10 V, R_G = 3.9 Ω, R_L = 0.5 Ω, I_{DS} = 50 A	-	25	-	nS
t_r	Turn-on Rise Time		-	177	-	
t_d(off)	Turn-off Delay Time		-	223	-	
t_f	Turn-off Fall Time		-	105	-	
Gate Charge Characteristics[Note4]						
Q_g	Total Gate Charge	V_{DS} = 15 V, V_{GS} = 10 V, I_{DS} = 50 A	-	266	-	nC
Q_{gs}	Gate-Source Charge		-	55	-	
Q_{gd}	Gate-Drain Charge		-	40	-	

Note 1：Limitation by silicon chip.
Note 2：Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
Note 3：Surface Mounted on 1 in^2 pad area, t ≤ 10 sec.
Note 4：Guaranteed by design, not subject to production testing.

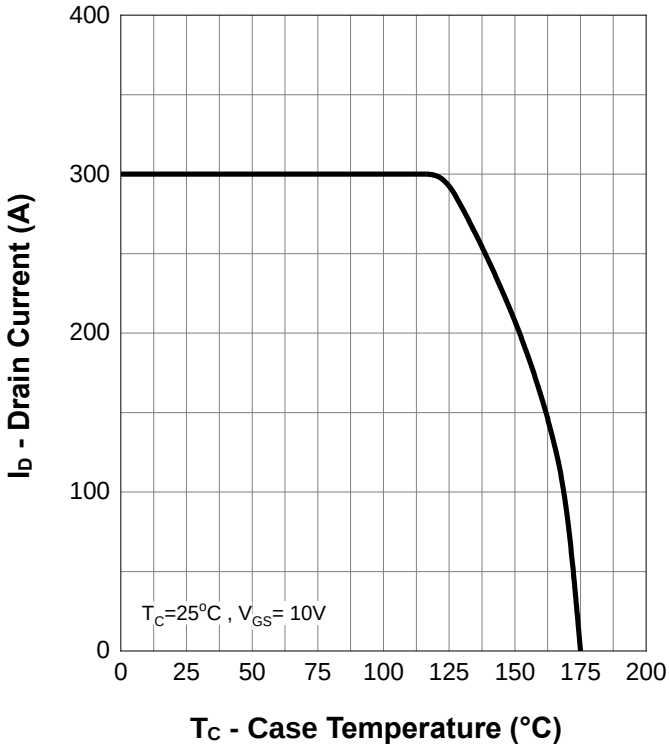
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6. Typical Characteristics

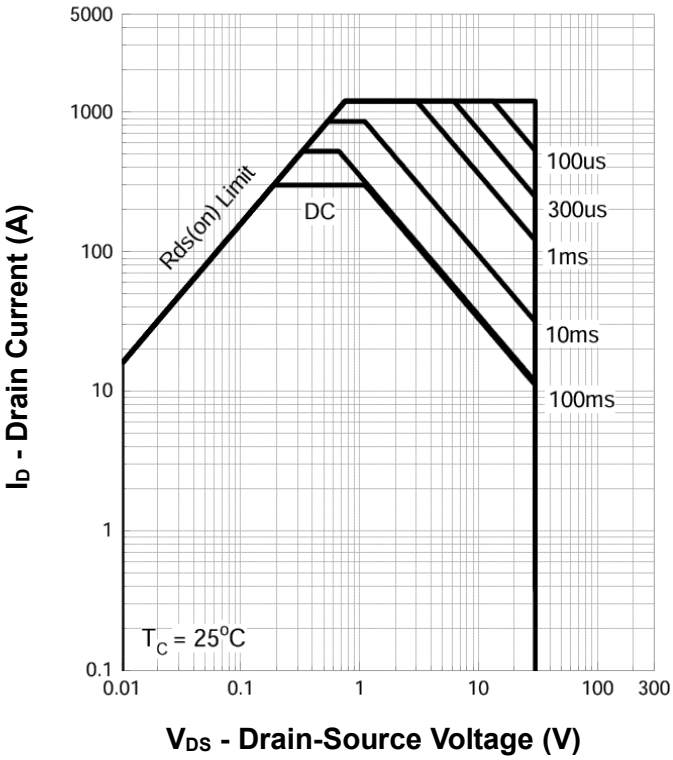
Power Capability



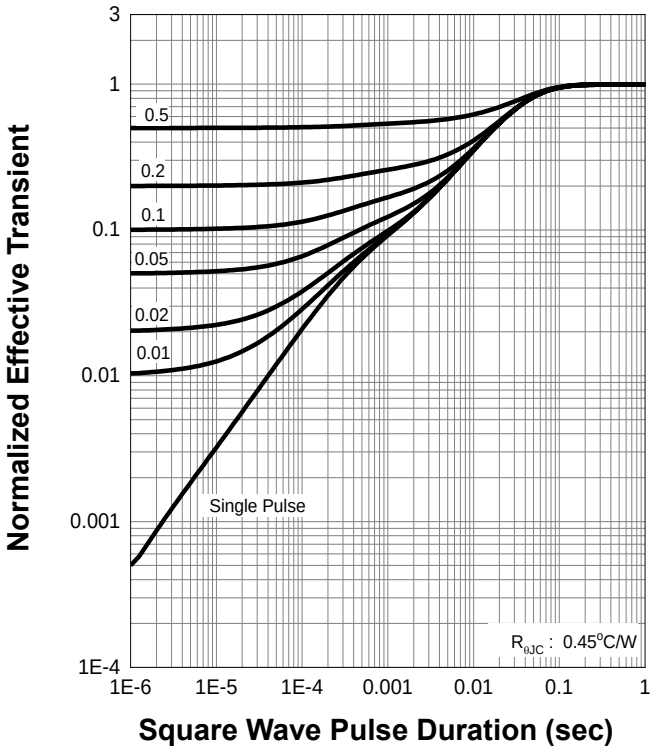
Current Capability



Safe Operating Area



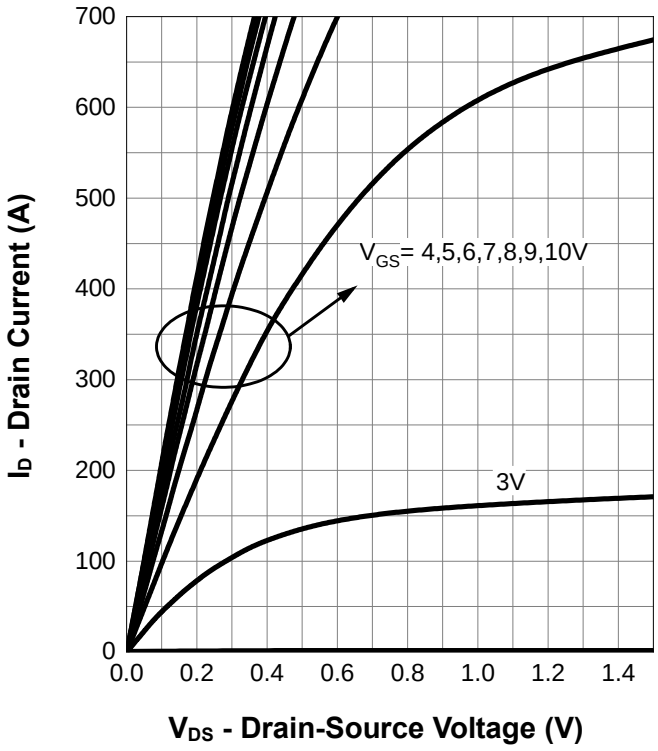
Transient Thermal Impedance



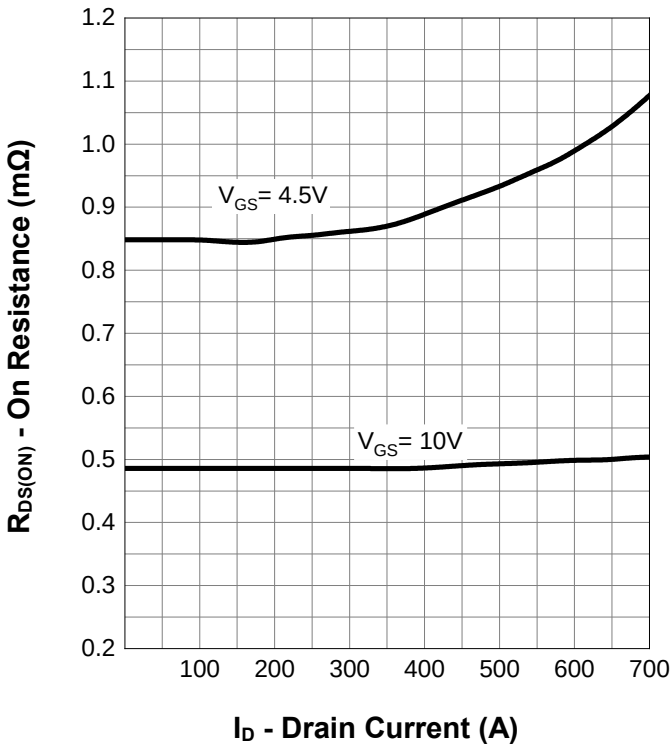
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6. Typical Characteristics (cont.)

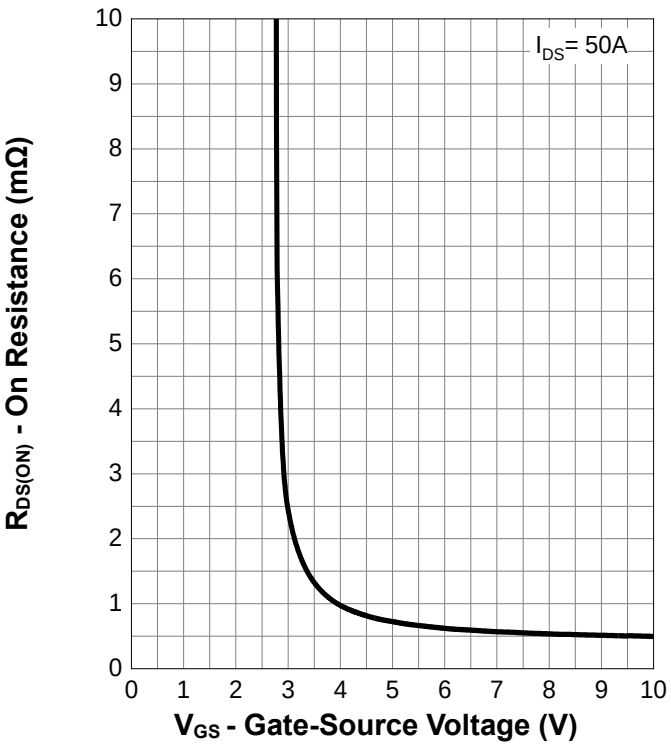
Output Characteristics



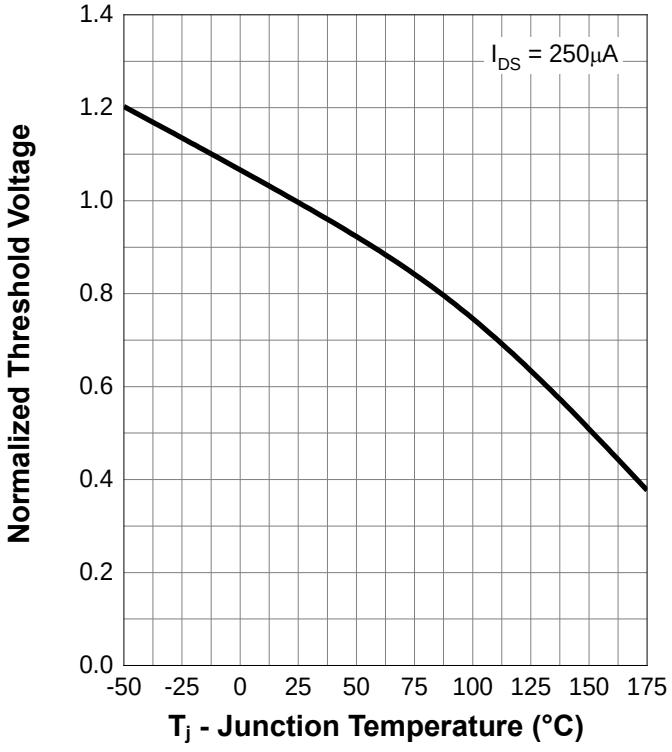
On Resistance



Transfer Characteristics



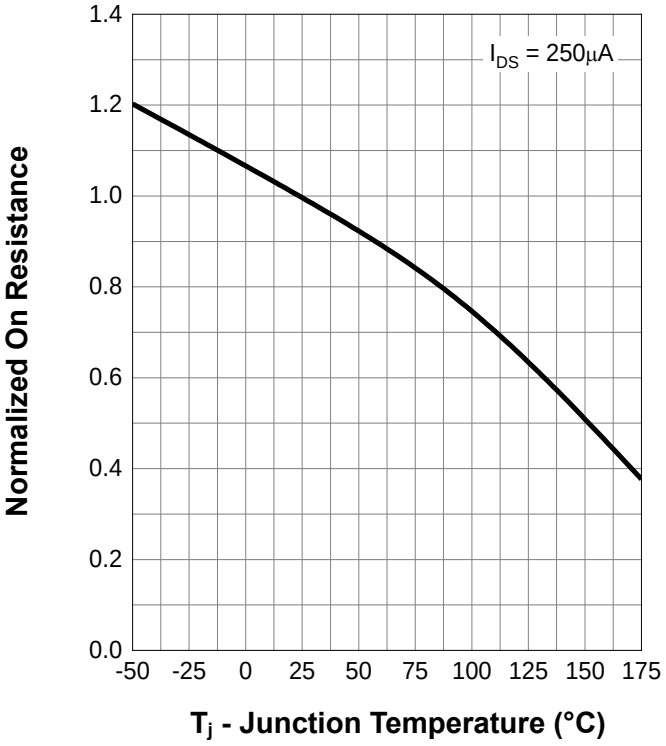
Normalized Threshold Voltage



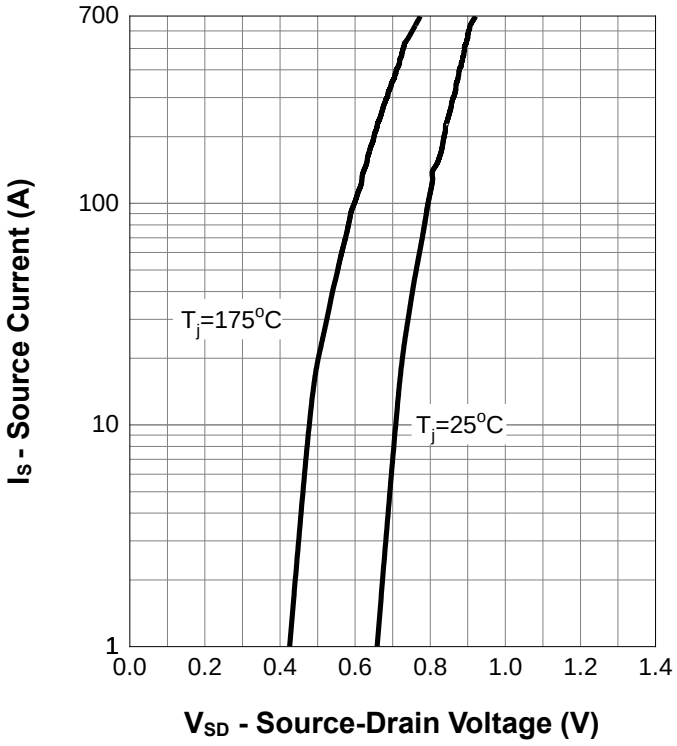
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6. Typical Characteristics (cont.)

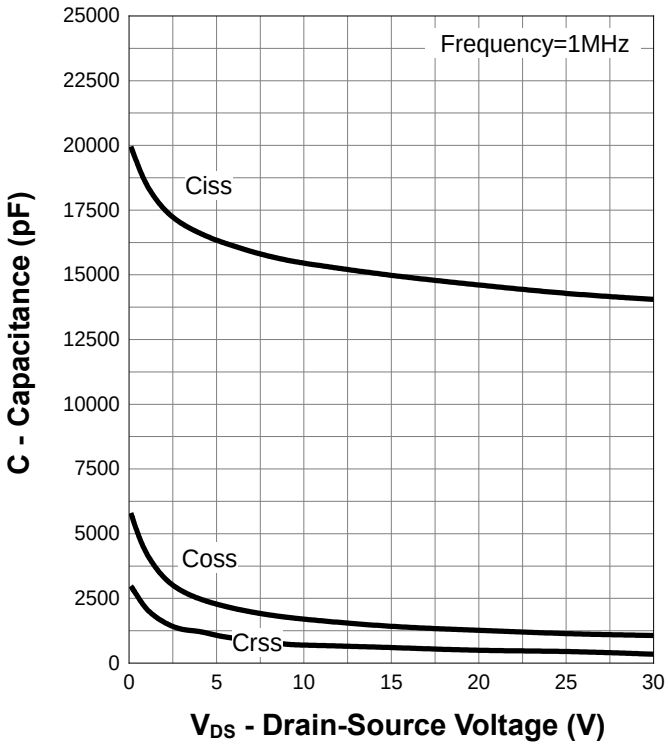
Normalized On Resistance



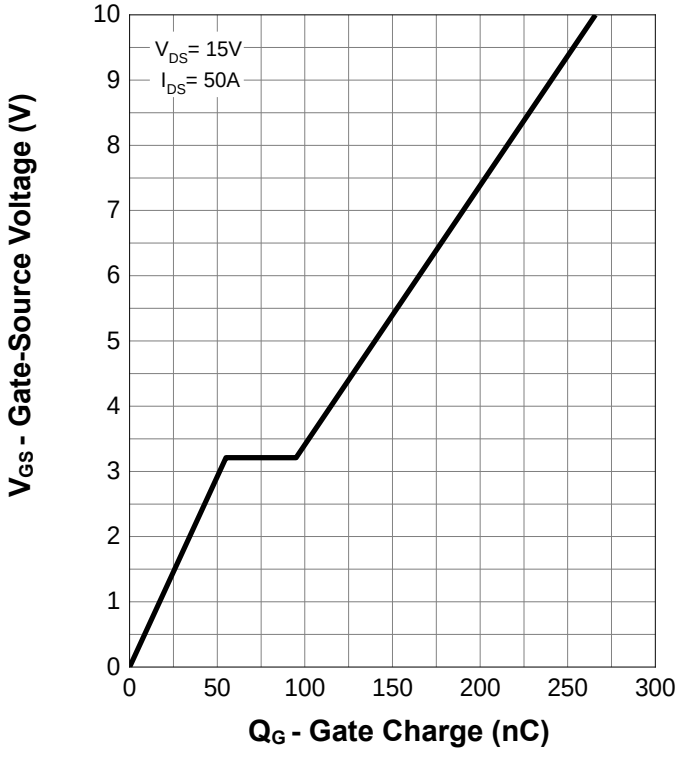
Diode Forward Current



Capacitance



Gate Charge



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