iM7127

N-Channel Enhancement Mode MOSFET

Preliminary Datasheet

1. Product Information

1.1 Features

- Advanced Trench Cell Design
- RoHS Compliant and Halogen Free
- Reliable and Rugged



1.2 Package Type

TOLLB-8L

1.3 Quick Reference

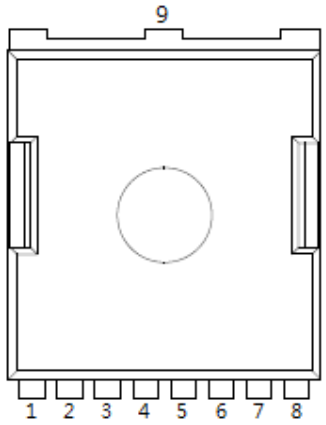
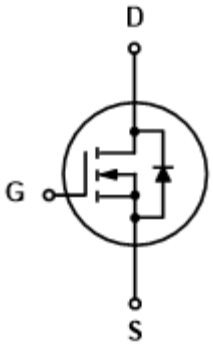
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Limiting Values						
P_{tot}	Total Power Dissipation	T_C = 25 ℃	-	-	186	W
I_D Note1	Drain Current	T_C = 25 ℃, V_{GS} = 10 V	-	-	120	A
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown	V_{GS} = 0 V, I_{DS} = 250 μA	100	-	-	V
$R_{DS(ON)}$	On-State Resistance	V_{GS} = 10 V, I_{DS} = 50 A	-	2.9	3.6	mΩ
		V_{GS} = 6 V, I_{DS} = 30 A	-	3.9	5.3	

2. Ordering Code & Marking Information

Ordering Code	Marking Information
iM7127	iM7127 XXXXX X : Date Code

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3. Pin Description

Pin	Description	Simplified Outline	Symbol
1	Gate(G)		
2~8	Source(S)		
9	Drain(D)		

4. Limiting Values

Symbol	Parameter		Rating	Unit
V_{DS}	Drain-Source Voltage		100	V
V_{GS}	Gate-Source Voltage		± 20	V
I_D	Drain Current	T_C = 25 ℃, V_{GS} = 10 V	120 Note1	A
		T_C = 100 ℃, V_{GS} = 10 V	103	A
		T_A = 25 ℃, V_{GS} = 10 V	20.2 Note2	A
		T_A = 100 ℃, V_{GS} = 10 V	12.7	A
I_{DM}	Pulsed Source Current	T_C = 25 ℃, V_{GS} = 10 V	480 Note3	A
		T_A = 25 ℃, V_{GS} = 10 V	81 Note2	A
I_S Note1	Diode Forward Current	T_C = 25 ℃, V_{GS} = 0 V	120	A
E_{AS}	Single Pulsed Avalanche Energy	L = 1.0 mH, V_{DD} = 50 V	450	mJ
P_{tot}	Total Power Dissipation	T_C = 25 ℃	186	W
$R_{\theta JA}$ Note2	Thermal Resistance- Junction to Ambient		45	℃ / W
$R_{\theta JC}$	Thermal Resistance- Junction to Case		0.67	℃ / W
T_{stg}	Storage Temperature		- 55~150	℃
T_J	Junction Temperature		150	℃

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5. Electrical Characteristics (T_A = 25 °C Unless Otherwise Noted)

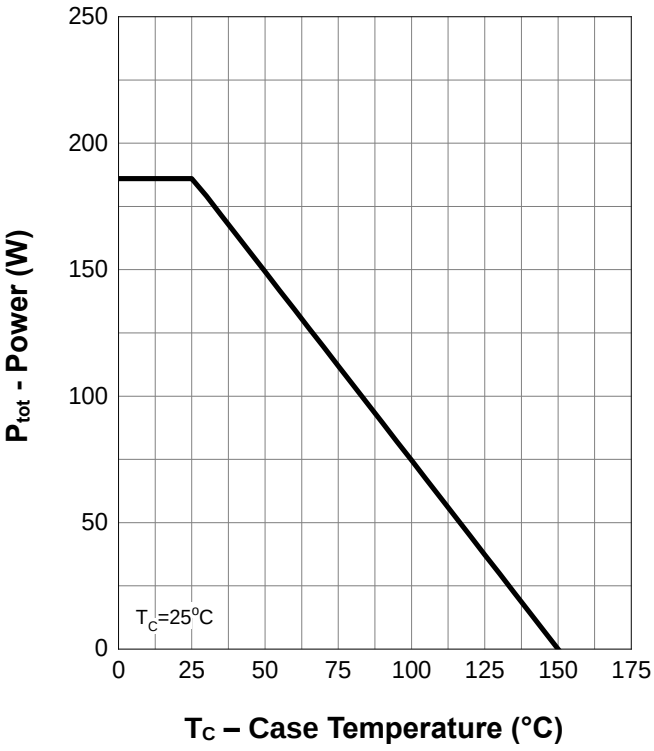
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown	V_{GS} = 0 V, I_{DS} = 250 μA	100	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250 μA	2	-	4	V
I_{DSS}	Drain Leakage Current	V_{DS} = 80 V, V_{GS} = 0 V	-	-	1	μA
I_{GSS}	Gate Leakage Current	V_{DS} = 0 V, V_{GS} = ± 20 V	-	-	±100	nA
$R_{DS(ON)}$	On-State Resistance	V_{GS} = 10 V, I_{DS} = 50 A	-	2.9	3.6	mΩ
		V_{GS} = 6 V, I_{DS} = 30 A	-	3.9	5.3	
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_{SD} = 50 A, V_{GS} = 0 V	-	-	1.3	V
t_{rr} Note4	Reverse Recovery Time	I_{SD} = 50 A, V_{GS} = 0 V	-	61	-	nS
Q_{rr} Note4	Reverse Recovery Charge	dI_{SD}/dt = 100 A/μs	-	82	-	nC
Dynamic Characteristics Note4						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 50 V Frequency = 1 MHz	-	5335	-	pF
C_{oss}	Output Capacitance		-	791	-	
C_{rss}	Reverse Transfer Capacitance		-	8	-	
t_d(on)	Turn-on Delay Time	V_{DS} = 50 V, V_{GEN} = 10 V, R_G = 3.9 Ω, R_L = 1Ω, I_{DS} = 50 A	-	19	-	nS
t_r	Turn-on Rise Time		-	71	-	
t_d(off)	Turn-off Delay Time		-	57	-	
t_f	Turn-off Fall Time		-	62	-	
Gate Charge Characteristics Note4						
Q_g	Total Gate Charge	V_{DS} = 50 V, V_{GS} = 10 V, I_{DS} = 50 A	-	95	-	nC
Q_{gs}	Gate-Source Charge		-	30	-	
Q_{gd}	Gate-Drain Charge		-	25	-	

Note 1: Limited by bonding wire.
Note 2: Surface Mounted on 1 in^2 pad area, t ≤ 10 sec.
Note 3: Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
Note 4: Guaranteed by design, not subject to production testing.

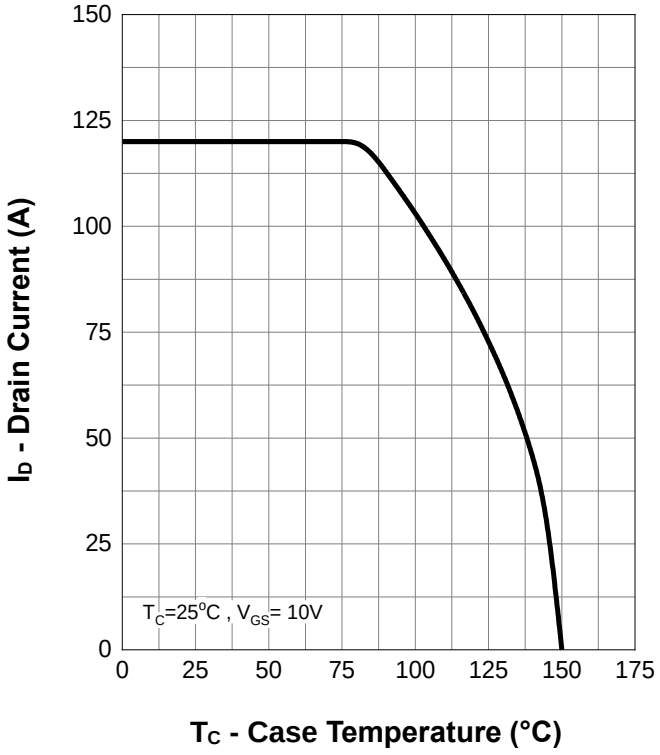
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6. Typical Characteristics

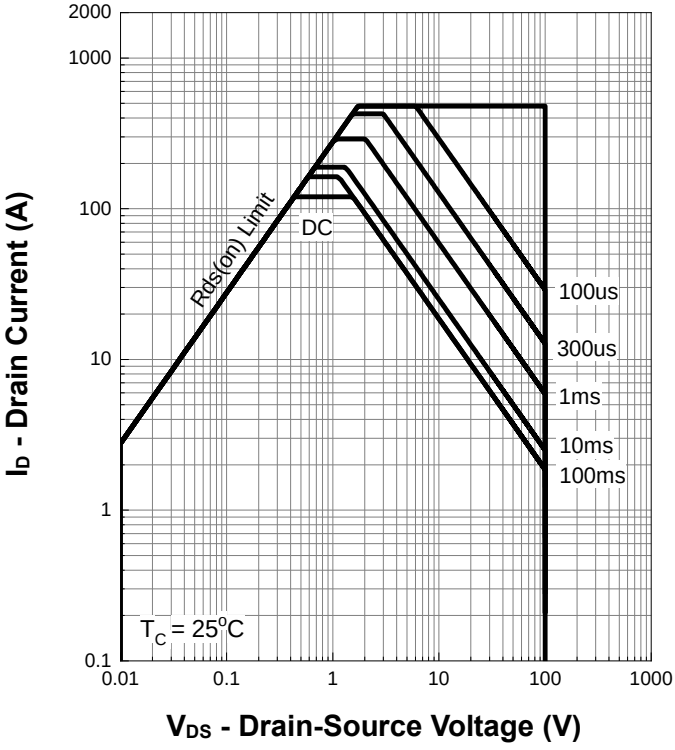
Power Capability



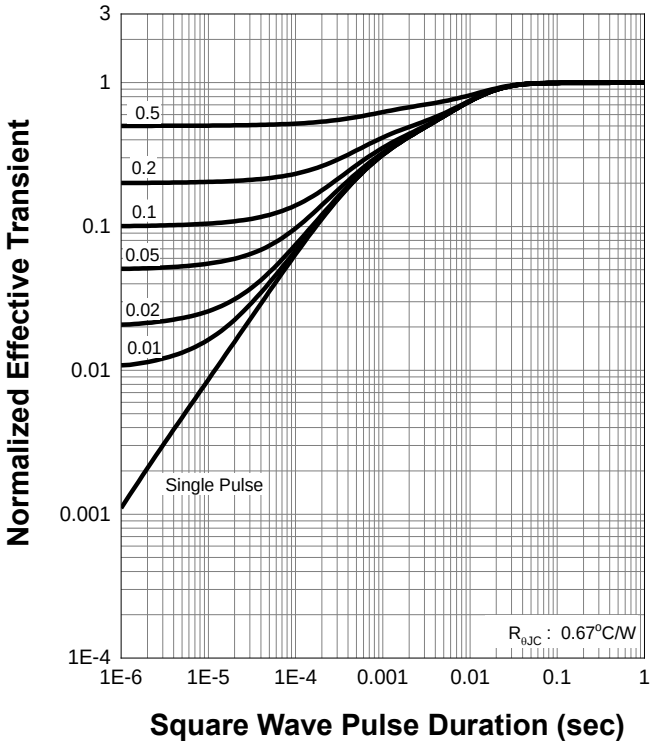
Current Capability



Safe Operating Area



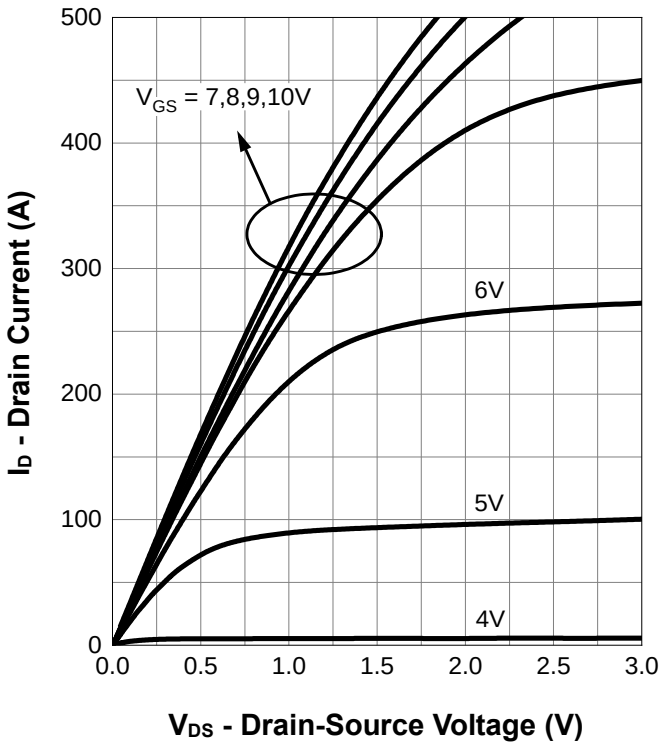
Transient Thermal Impedance



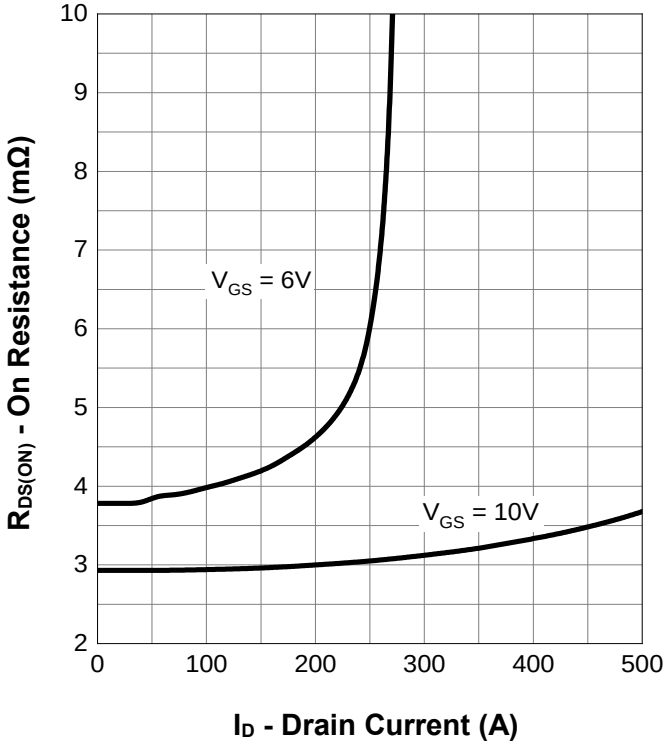
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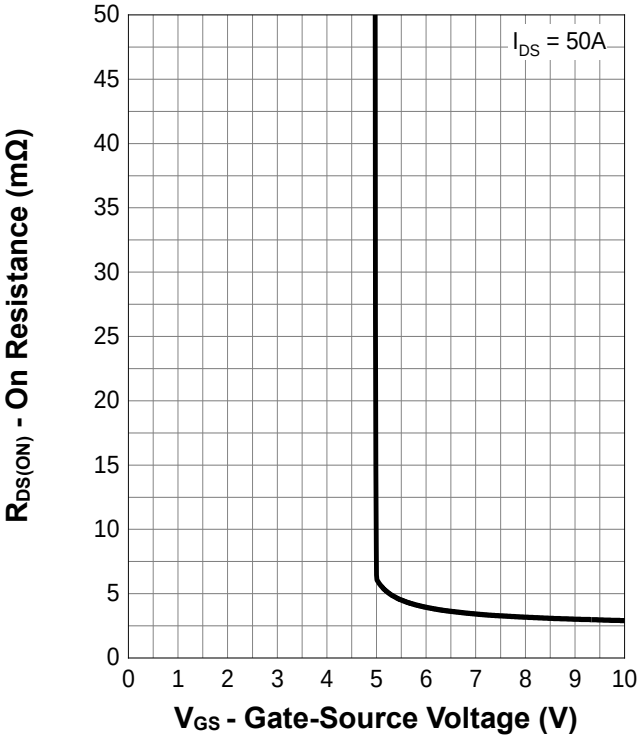
Output Characteristics



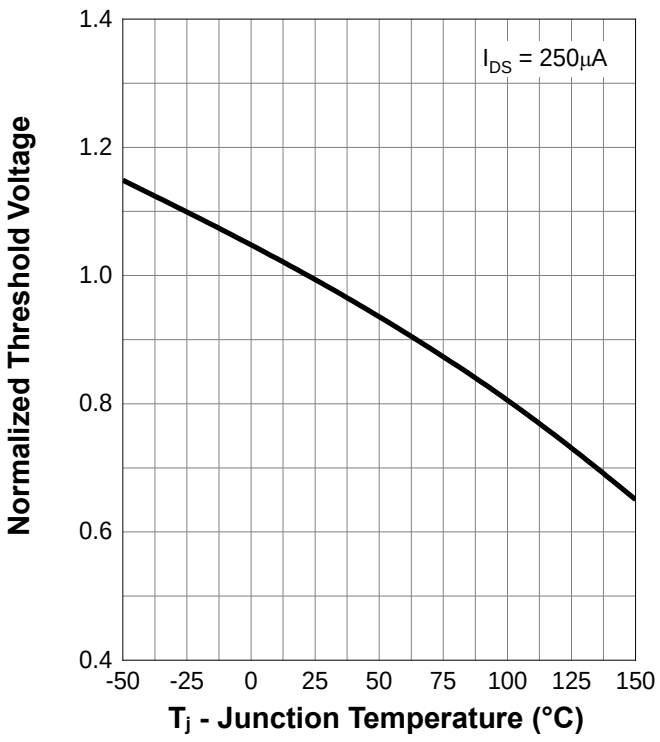
On Resistance



Transfer Characteristics



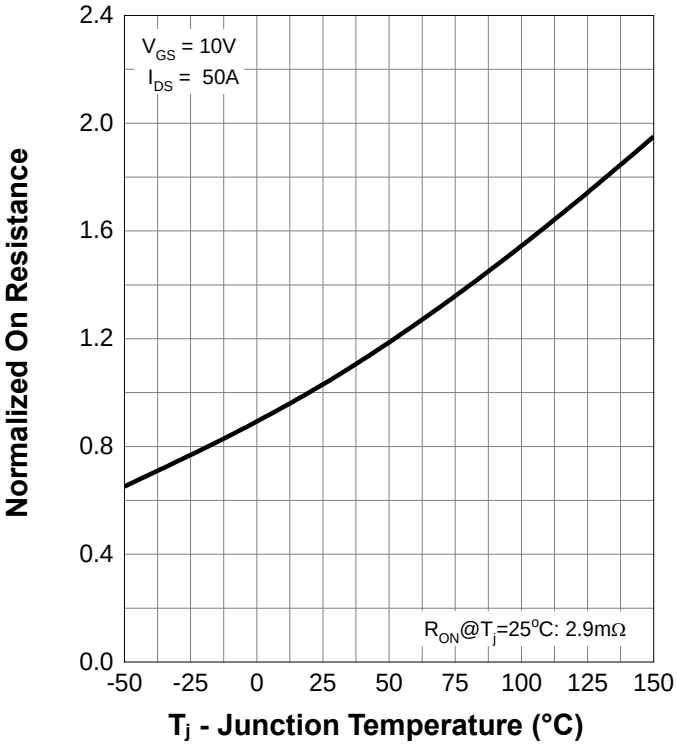
Normalized Threshold Voltage



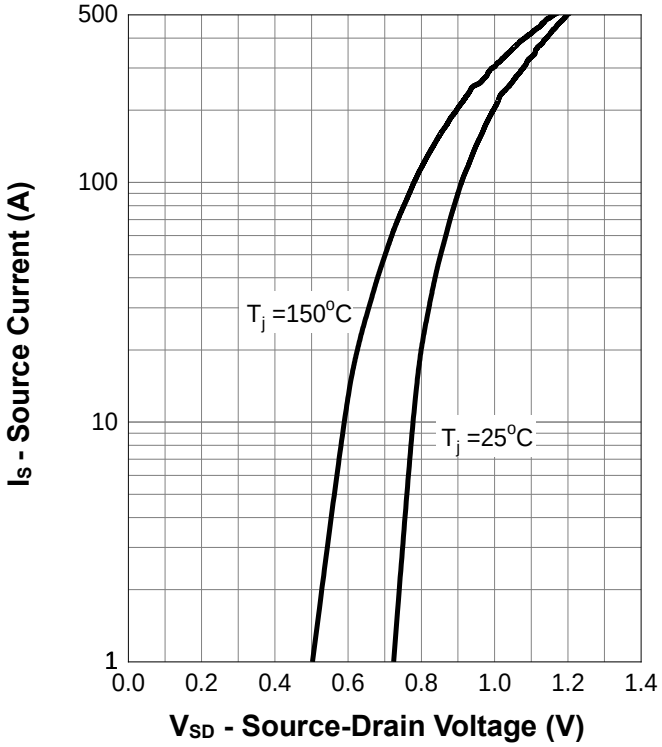
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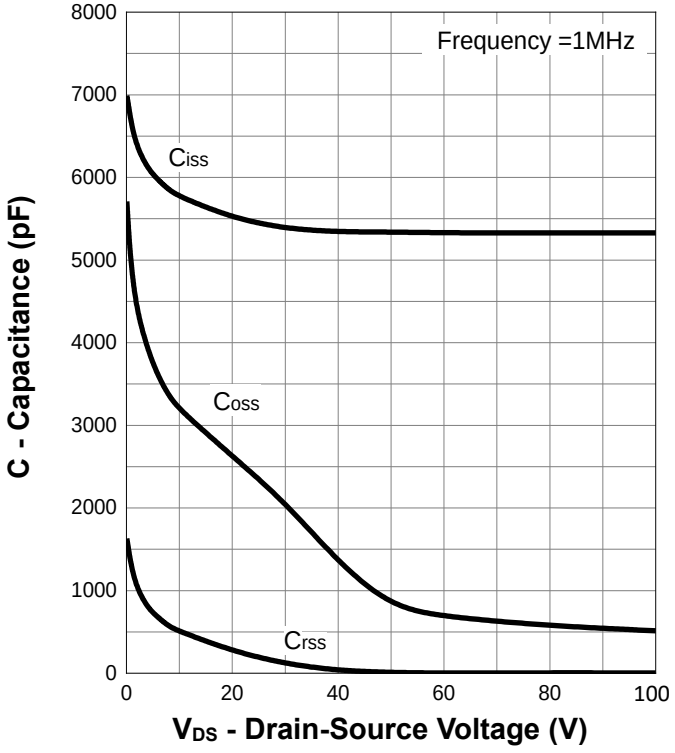
Normalized On Resistance



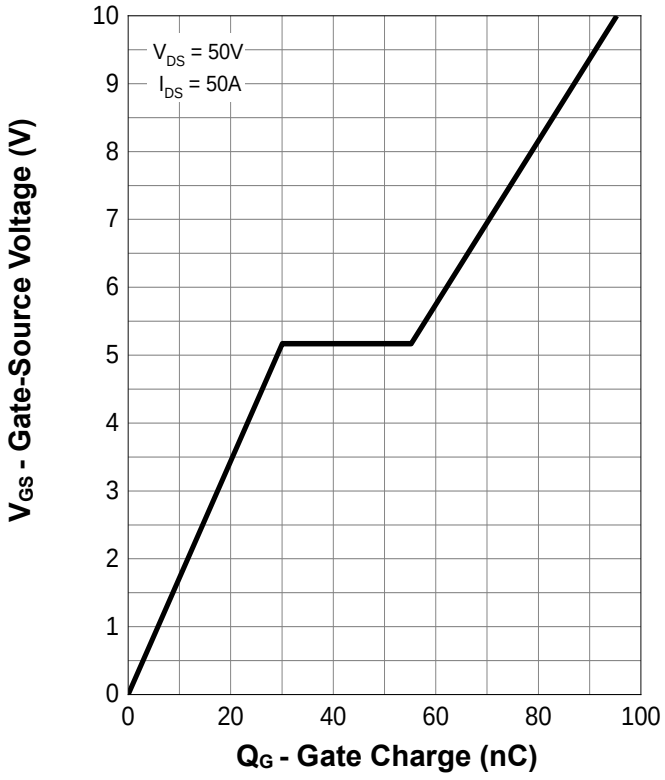
Diode Forward Current



Capacitance



Gate Charge



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