iM6239

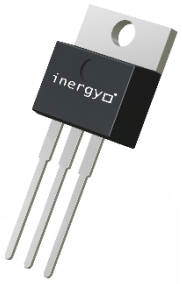
N-Channel Enhancement Mode MOSFET

Datasheet

1. Product Information

1.1 Features

- Advanced Trench Cell Design
- RoHS Compliant and Halogen Free
- Reliable and Rugged



1.2 Package Type

TO220A-3L

1.3 Quick Reference

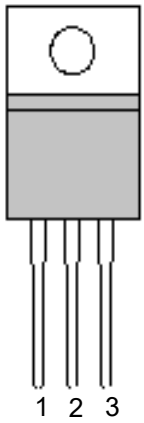
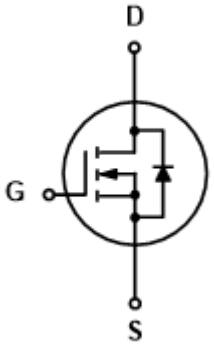
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Limiting Values						
P_{tot}	Total Power Dissipation	T_C = 25 ℃	-	-	500	W
I_{DS} Note1	Drain-Source Current	T_C = 25 ℃, V_{GS} = 10 V	-	-	120	A
		T_C = 100 ℃, V_{GS} = 10 V	-	-	102	
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 250 μA	200	-	-	V
$V_{GS(th)}$	Gate-Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250 μA	2	-	4	
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS} = 10 V, I_{DS} = 30 A	-	7	8.7	mΩ
		V_{GS} = 6 V, I_{DS} = 20 A	-	7.7	10.4	

2. Ordering Code & Marking Information

Ordering Code	Marking Information
iM6239	iM6239 XXXXX X: Date Code

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3. Pin Description

Pin	Description	Simplified Outline	Symbol
1	Gate (G)		
2	Drain (D)		
3	Source (S)		

4. Limiting Values

Symbol	Parameter		Rating	Unit
V_{DS}	Drain-Source Voltage		200	V
V_{GS}	Gate-Source Voltage		± 20	
I_{DS} Note1	Drain-Source Current	T_C = 25 ℃, V_{GS} = 10 V	120	A
		T_C = 100 ℃, V_{GS} = 10 V	102	
I_{DM} Note2	Pulsed Drain-Source Current	T_C = 25 ℃, V_{GS} = 10 V	400	A
I_S	Diode Forward Current	T_C = 25 ℃, V_{GS} = 0 V	120	
E_{AS}	Single Pulsed Avalanche Energy	L = 1.0 mH, V_{DD} = 50 V	1512	mJ
P_{tot}	Total Power Dissipation	T_C = 25 ℃	500	W
$R_{\theta JA}$ Note3	Thermal Resistance- Junction to Ambient		41	℃ / W
$R_{\theta JC}$	Thermal Resistance- Junction to Case		0.25	
T_{stg}	Storage Temperature		- 55 ~ 150	℃
T_J	Junction Temperature		150	

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5. Electrical Characteristics (T_A = 25 °C Unless Otherwise Noted)

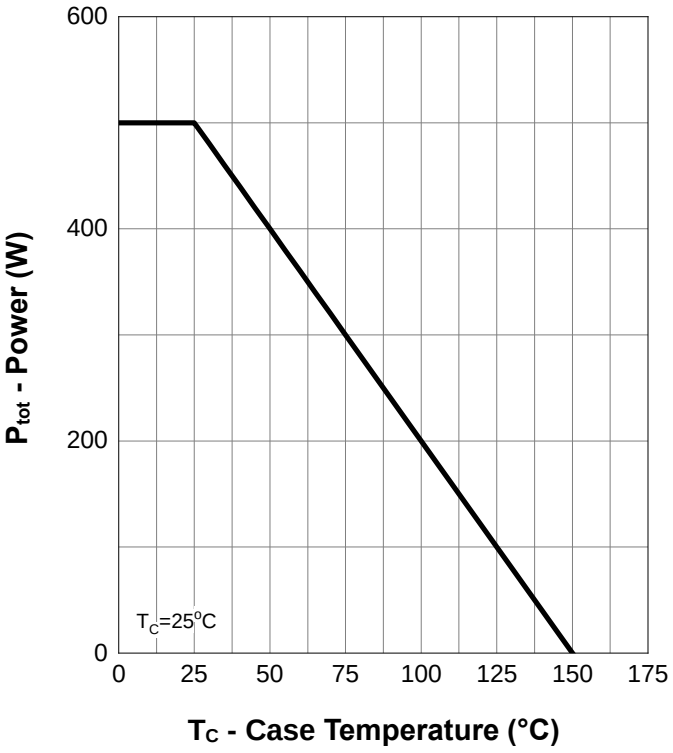
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 250 μA	200	-	-	V
$V_{GS(th)}$	Gate-Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250 μA	2	-	4	
I_{DSS}	Drain Leakage Current	V_{DS} = 160 V, V_{GS} = 0 V	-	-	1	μA
I_{GSS}	Gate Leakage Current	V_{DS} = 0 V, V_{GS} = ± 20 V	-	-	±100	nA
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS} = 10 V, I_{DS} = 30 A	-	7	8.7	mΩ
		V_{GS} = 6 V, I_{DS} = 20 A	-	7.7	10.4	
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_{SD} = 30 A, V_{GS} = 0 V	-	-	1.3	V
t_{rr} Note4	Reverse Recovery Time	I_{DS} = 30 A, V_{GS} = 0 V dI_{SD}/dt = 100 A/μs	-	125	-	nS
Q_{rr} Note4	Reverse Recovery Charge		-	772	-	nC
Dynamic Characteristics Note4						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 100 V Frequency = 1 MHz	-	9388	-	pF
C_{oss}	Output Capacitance		-	474	-	
C_{rss}	Reverse Transfer Capacitance		-	51	-	
t_d(on)	Turn-on Delay Time	V_{DS} = 100 V, V_{GEN} = 10 V, R_G = 3.9 Ω, R_L = 3.3 Ω, I_{DS} = 30 A	-	26	-	nS
t_r	Turn-on Rise Time		-	87	-	
t_d(off)	Turn-off Delay Time		-	102	-	
t_f	Turn-off Fall Time		-	81	-	
Gate Charge Characteristics Note4						
Q_g	Total Gate Charge	V_{DS} = 100 V, V_{GS} = 10 V, I_{DS} = 30 A	-	149	-	nC
Q_{gs}	Gate-Source Charge		-	48	-	
Q_{gd}	Gate-Drain Charge		-	33	-	

Note 1: Limitation by silicon chip.
Note 2: Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
Note 3: Surface Mounted on 1 in^2 pad area, t ≤ 10 sec.
Note 4: Guaranteed by design, not subject to production testing.

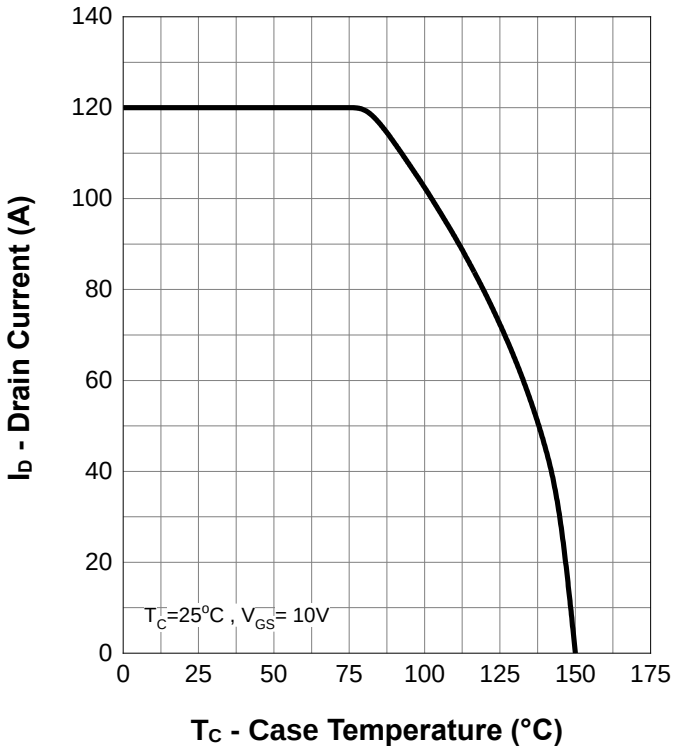
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6. Electrical Characteristics

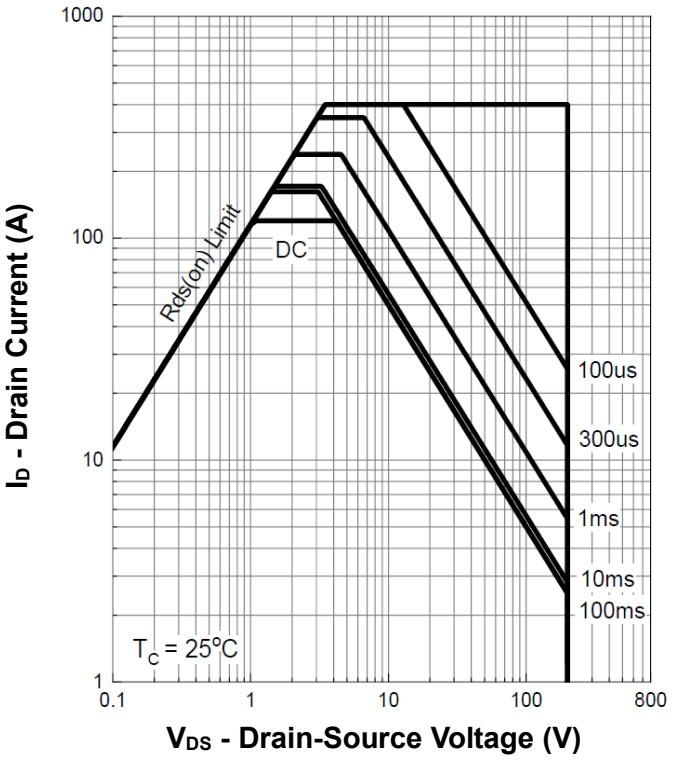
Power Capability



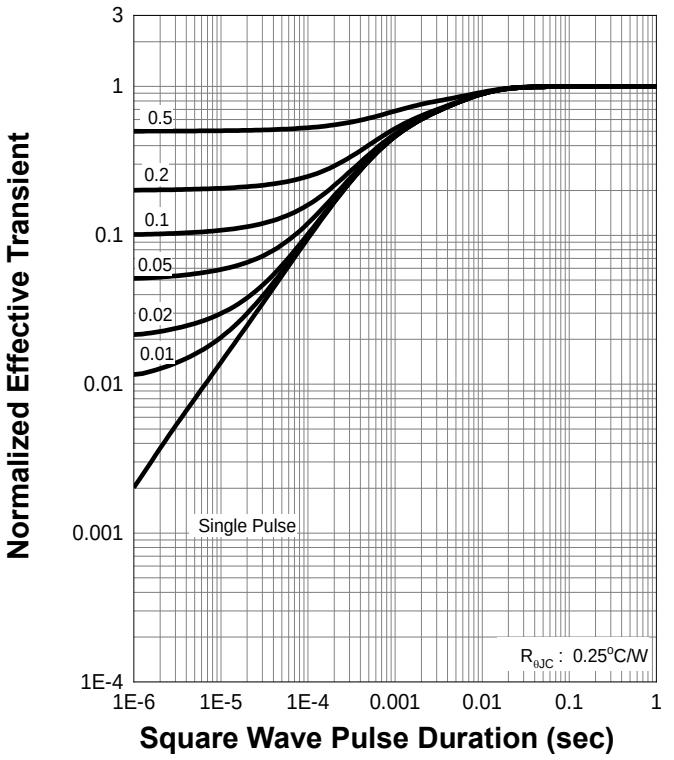
Current Capability



Safe Operating Area



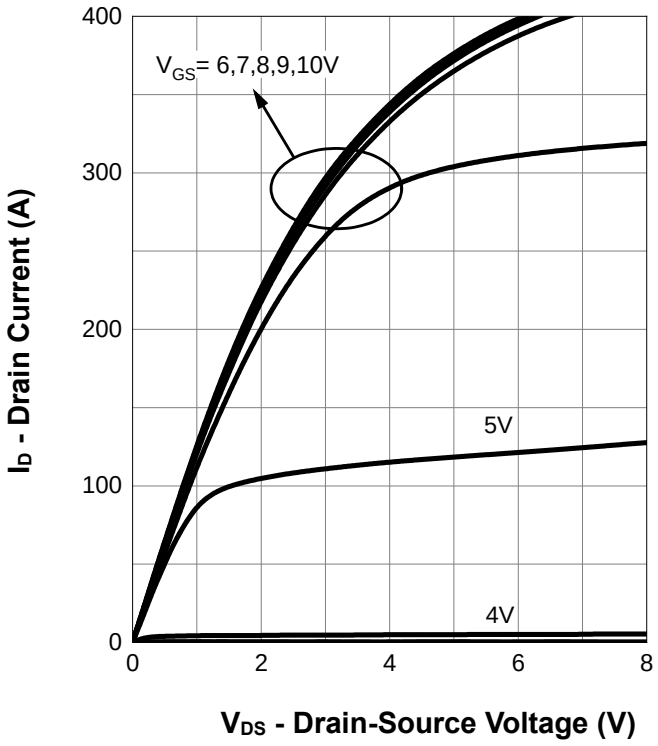
Transient Thermal Impedance



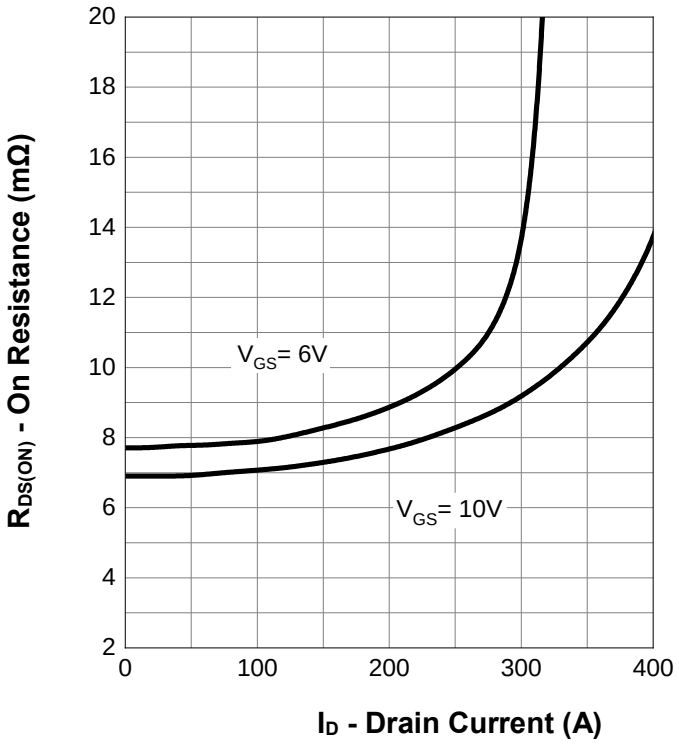
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6. Electrical Characteristics (cont.)

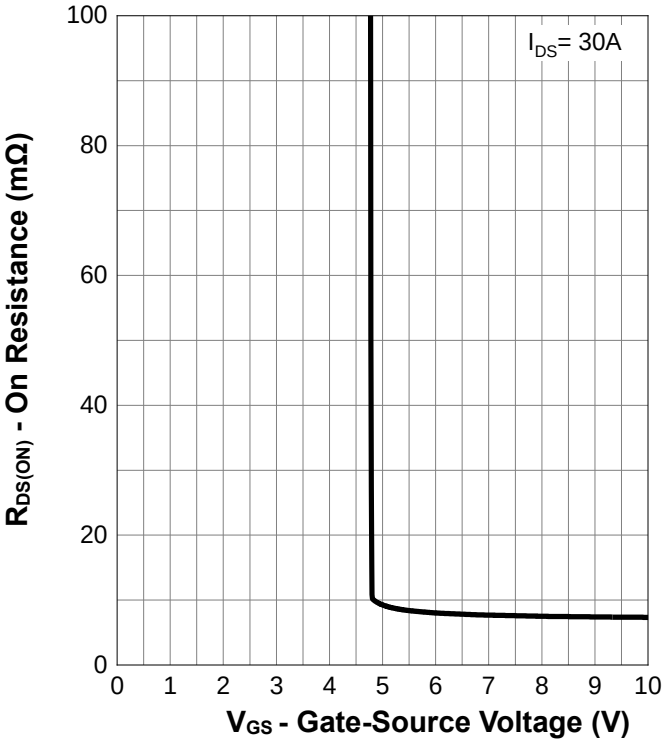
Output Characteristics



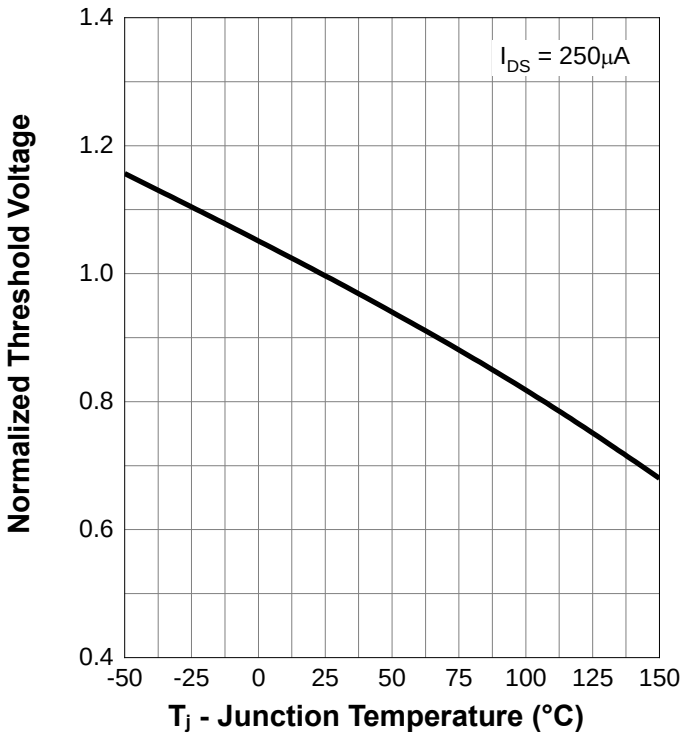
On Resistance



Transfer Characteristics



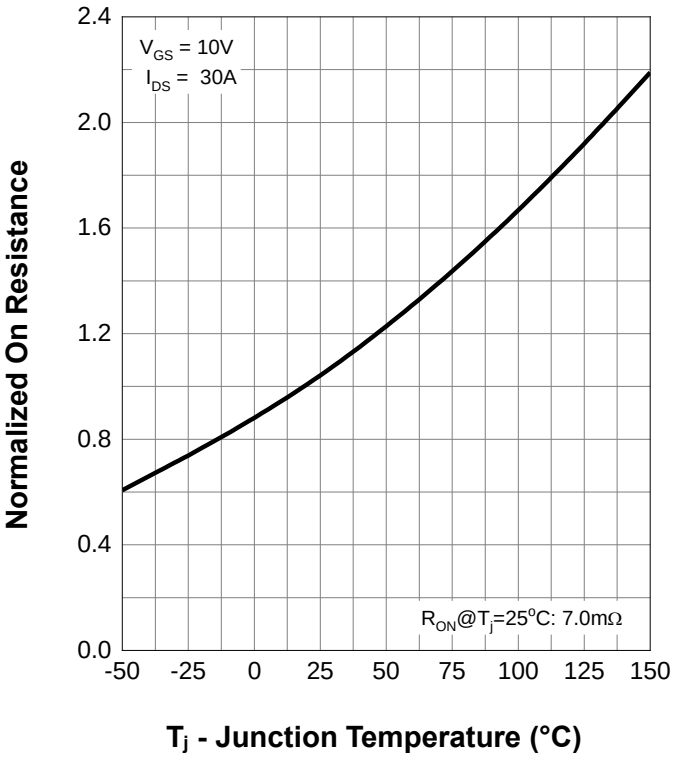
Normalized Threshold Voltage



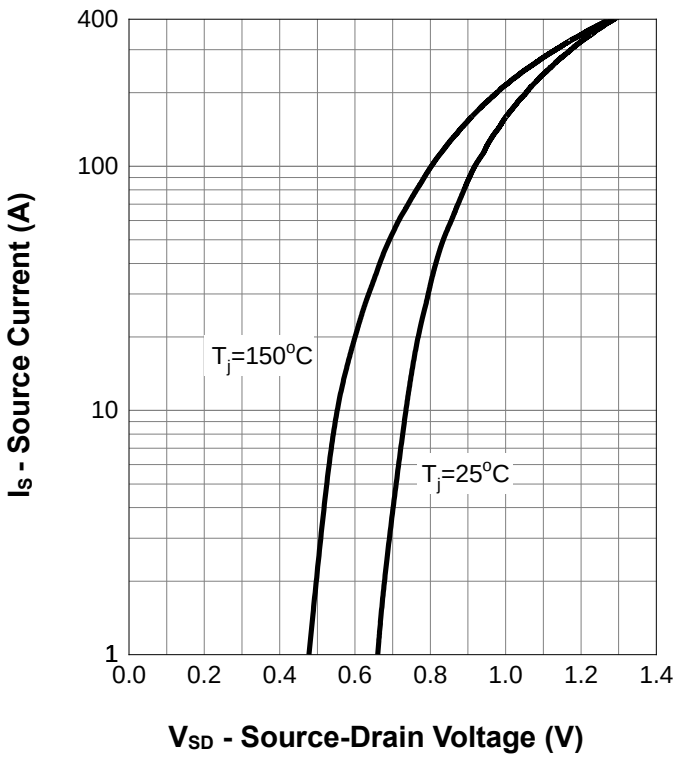
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6. Typical Characteristics (cont.)

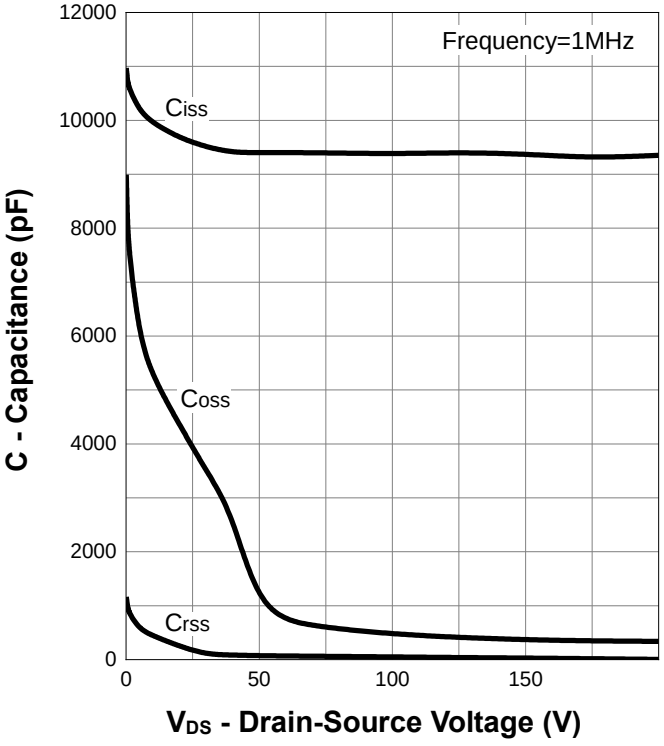
Normalized On Resistance



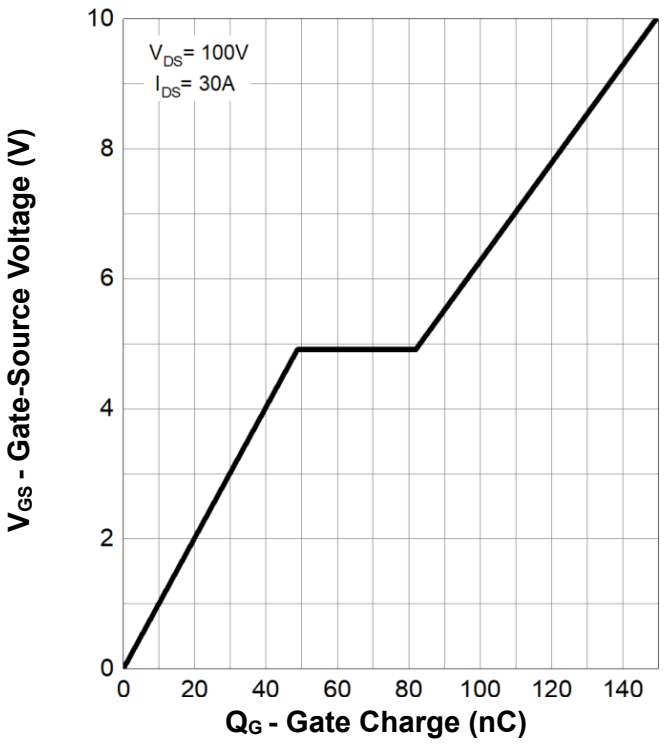
Diode Forward Current



Capacitance



Gate Charge



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