iM2312

P-Channel Enhancement Mode MOSFET

Datasheet

1. Product Information

1.1 Features

- Advanced Trench Cell Design
- RoHS Compliant and Halogen Free
- Reliable and Rugged
- ESD Protection



1.2 Package Type

SOT23-3L

1.3 Quick Reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Limiting Values						
P_{tot}	Total Power Dissipation	T_C = 25 ℃	-	-	0.98	W
I_D	Drain Current	T_C = 25 ℃, V_{GS} = -4.5 V	-	-	-3.3	A
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown	V_{GS} = 0 V, I_{DS} = -250 μA	-30	-	-	V
$R_{DS(ON)}$ Note2	On-State Resistance	V_{GS} = -4.5V, I_{DS} = -3 A	-	45	58	mΩ
		V_{GS} = -2.5V, I_{DS} = -2.5 A	-	60	90	
		V_{GS} = -1.8V, I_{DS} = -0.5 A	-	85	127	

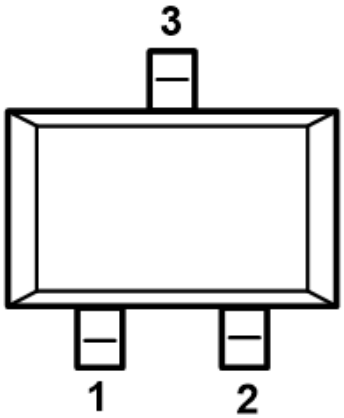
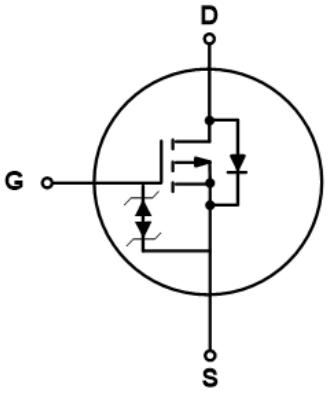
Note 1：Surface Mounted on 1 in^2 pad area, t ≤ 10 sec.
Note 2：Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
Note 3：Limited by bonding wire.

2. Ordering Code & Marking Information

Ordering Code	Marking Information
iM2312	312XX X : Date Code

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3. Pin Description

Pin	Description	Simplified Outline	Symbol
1	Gate		
2	Source		
3	Drain		

4. Limiting Values

Symbol	Parameter		Rating	Unit
V_{DS}	Drain-Source Voltage		-30	V
V_{GS}	Gate-Source Voltage		± 10	V
I_D	Drain Current	T_A= 25 ℃	-3.3	A
		T_A= 100 ℃	-2.1	A
I_{DM}	Pulsed Source Current	T_A = 25 ℃	-13	A
I_S	Diode Forward Current	T_A = 25 ℃	-3.3	A
E_{AS}	Single Pulsed Avalanche Energy	L= 1.0mH	36	mJ
P_{tot}	Total Power Dissipation	T_A = 25 ℃	0.98	W
$R_{\theta JA}$ Note1	Thermal Resistance- Junction to Ambient		128	℃ / W
T_{stg}	Storage Temperature		-55~150	℃
T_J	Junction Temperature		150	℃

Note 1：Surface Mounted on 1 in^2 pad area, t ≤ 10 sec.
Note 2：Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
Note 3：Limited by bonding wire.

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5. Electrical Characteristics (T_A = 25 °C Unless Otherwise Noted)

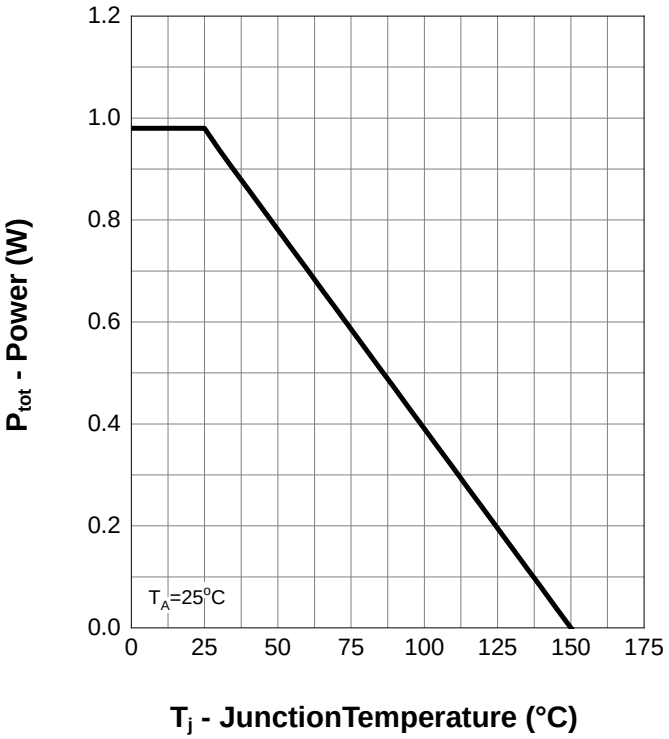
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = -250 μA	-30	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = -250 μA	-0.5	-	-1	V
I_{DSS}	Drain Leakage Current	V_{DS} = -24V, V_{GS} = 0 V	-	-	-1	μA
I_{GSS}	Gate Leakage Current	V_{DS} = 0 V, V_{GS} = ± 8 V	-	-	±10	uA
$R_{DS(ON)}$ Note1	On-State Resistance	V_{GS} = -4.5V, I_{DS} = -3A	-	45	58	mΩ
		V_{GS} = -2.5V, I_{DS} = -2.5 A	-	60	90	
		V_{GS} = -1.8V, I_{DS} = -0.5 A	-	85	127	
Diode Characteristics						
V_{SD} Note1	Diode Forward Voltage	I_{SD} = -3 A, V_{GS} = 0 V	-	-	1.3	V
t_{rr}	Reverse Recovery Time	I_{DS} = -3 A, V_{GS} = 0 V	-	44	-	nS
Q_{rr}	Reverse Recovery Charge	dI_{SD}/dt = 100 A/μs	-	17	-	nC
Dynamic Characteristics Note2						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = -15 V Frequency = 1 MHz	-	1095	-	pF
C_{oss}	Output Capacitance		-	89	-	
C_{rss}	Reverse Transfer Capacitance		-	83	-	
t_d(on)	Turn-on Delay Time	V_{DS} = -15 V, V_{GEN} = -4.5 V, R_G = 3.9 Ω, R_L =5Ω, I_{DS} = -3 A	-	4	-	nS
t_r	Turn-on Rise Time		-	19	-	
t_d(off)	Turn-off Delay Time		-	60	-	
t_f	Turn-off Fall Time		-	173	-	
Gate Charge Characteristics Note2						
Q_g	Total Gate Charge	V_{DS} = -15 V, V_{GS} = -4.5 V, I_{DS} = -3A	-	11	-	nC
Q_{gs}	Gate-Source Charge		-	3.9	-	
Q_{gd}	Gate-Drain Charge		-	2.6	-	

Note 1: Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
Note 2: Guaranteed by design, not subject to production testing.

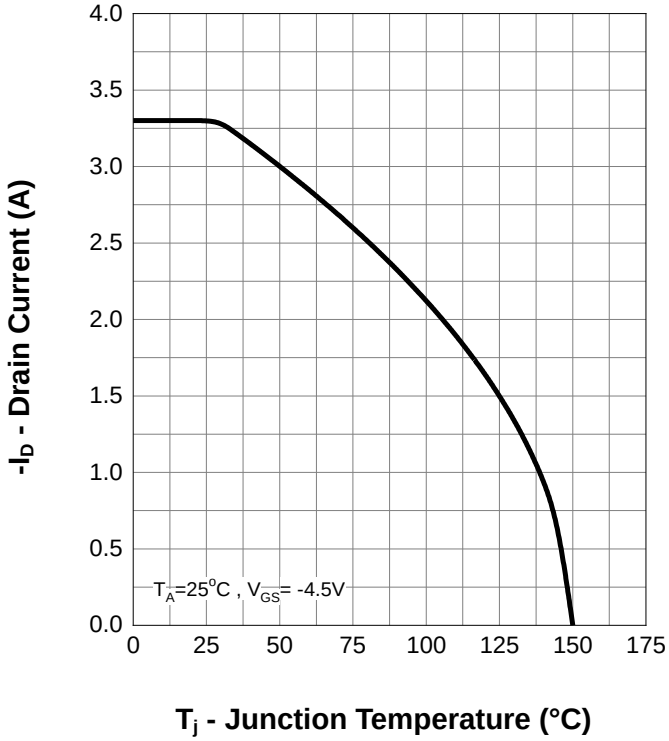
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6. Typical Characteristics

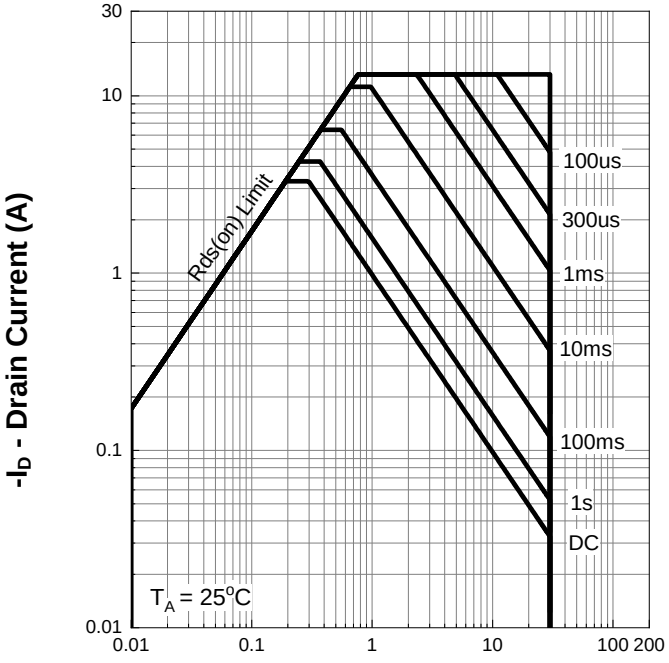
Power Capability



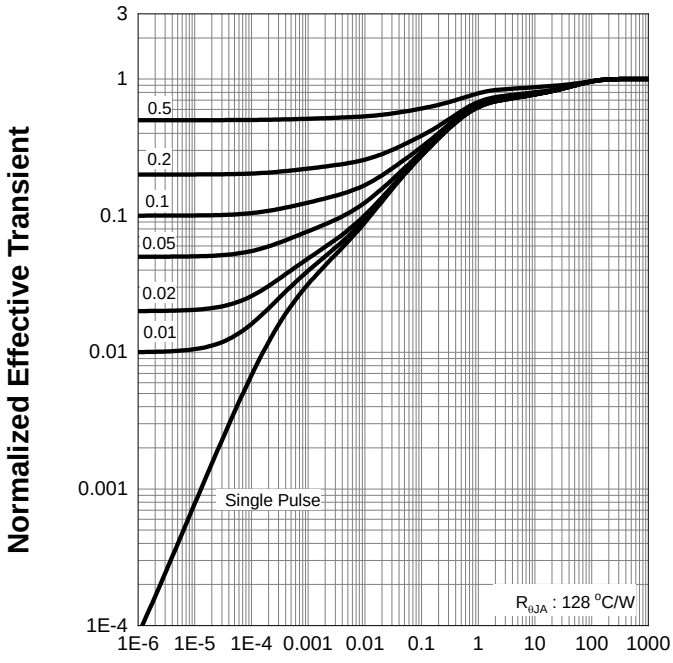
Current Capability



Safe Operating Area



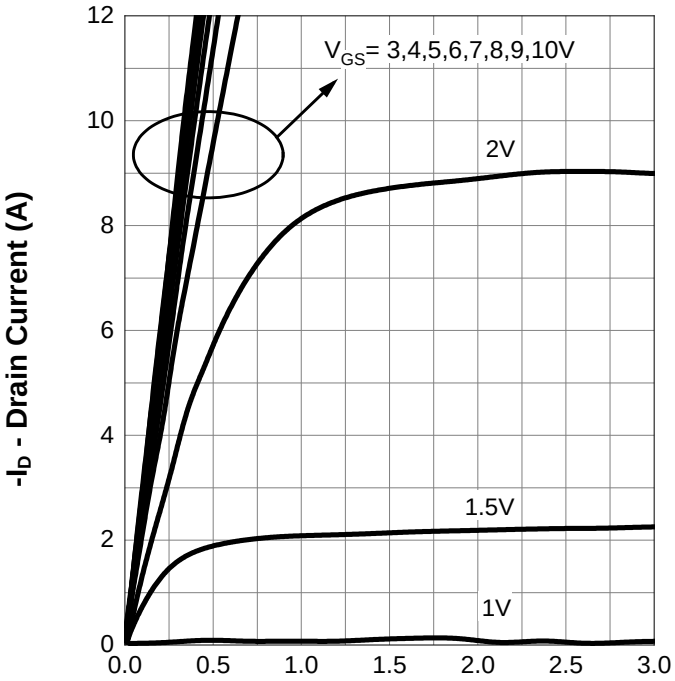
Transient Thermal Impedance



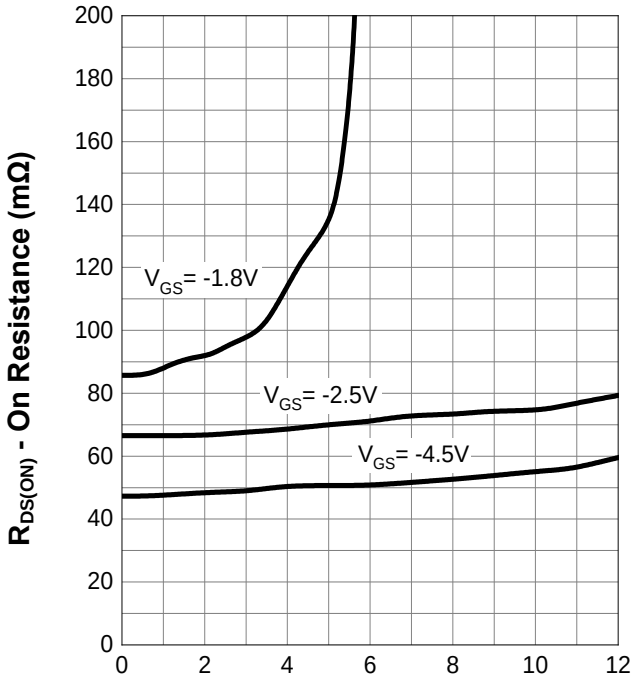
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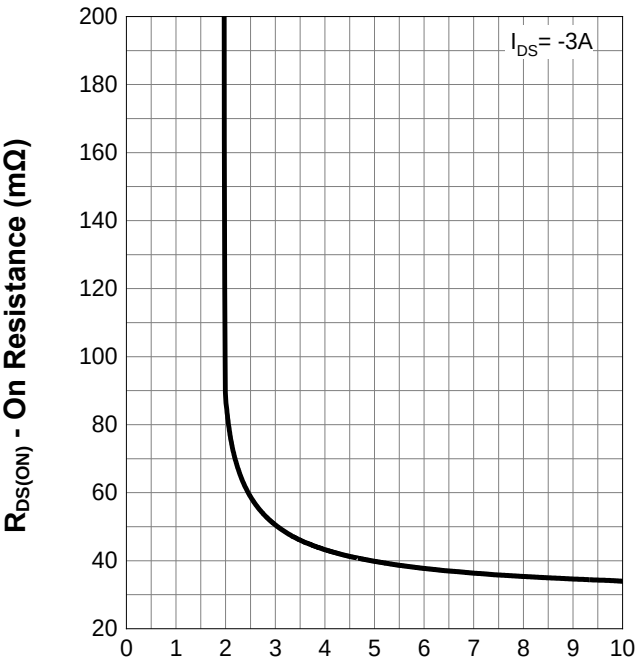
Output Characteristics



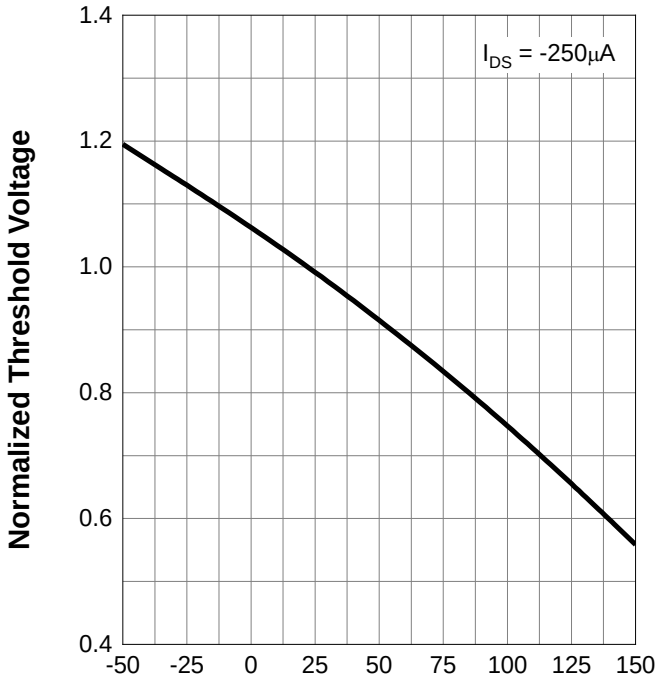
On Resistance



Transfer Characteristics



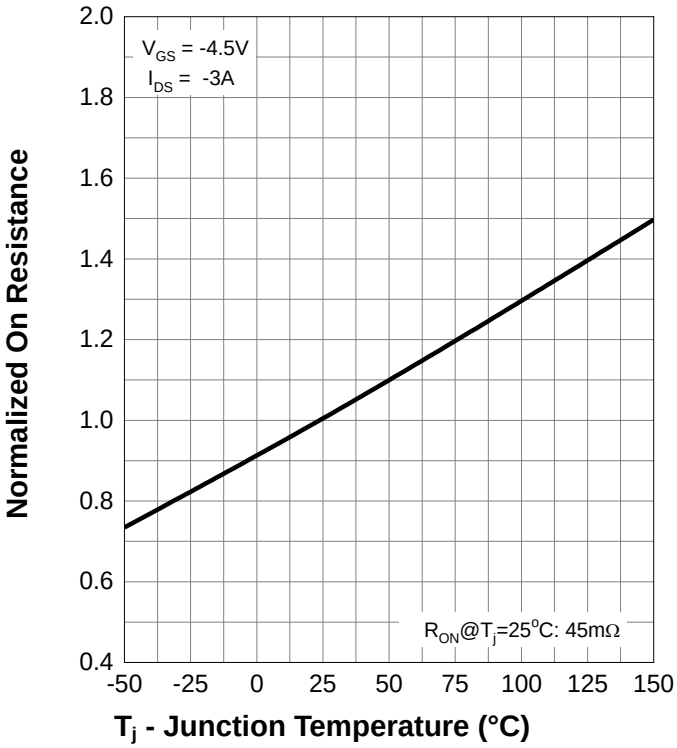
Normalized Threshold Voltage



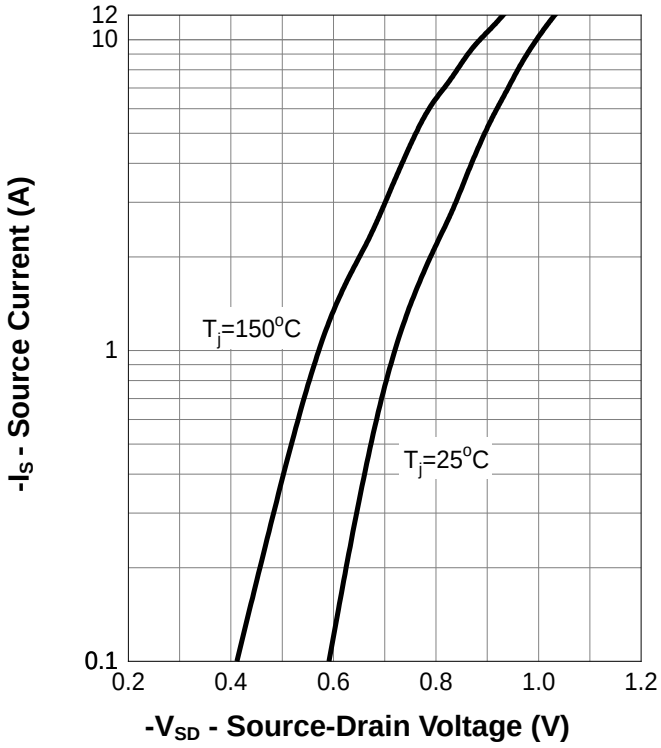
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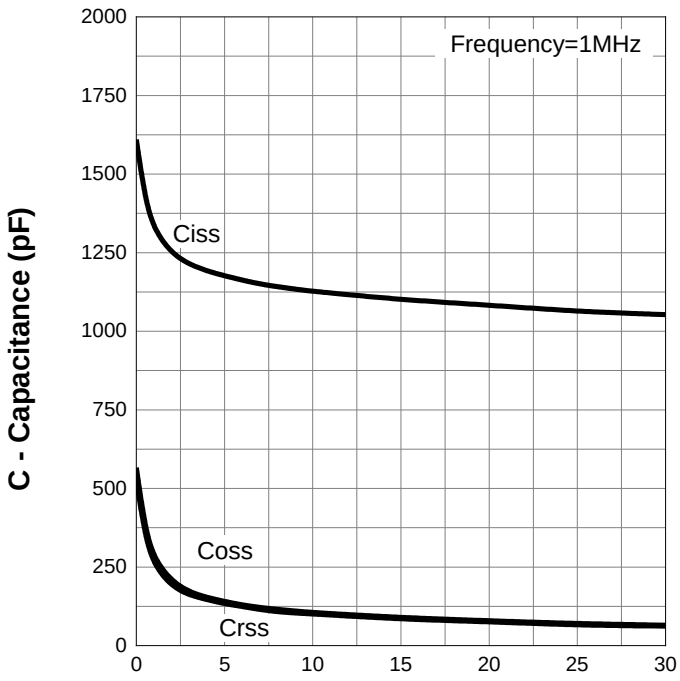
Normalized On Resistance



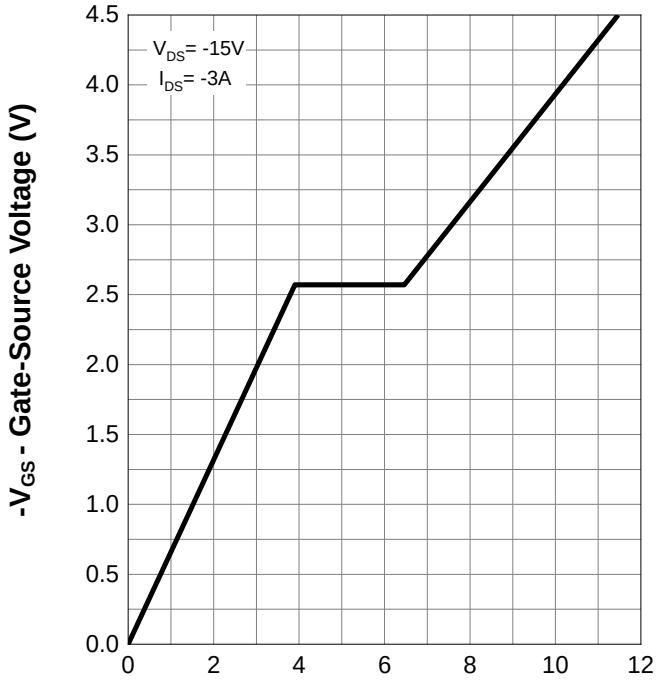
Diode Forward Current



Capacitance



Gate Charge



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