Transition-Mode PFC Controller with THD Enhanced

REV: 00

General Description

The LD7597A is a current mode PFC controller operating on critical conduction (CRM) or discontinuous (DCM) mode. It built in THDi improved circuit for all operating mode. It's based on DCM operation with frequency limitation method to improve the efficiency at light load condition.

The device is also integrated several functions of protection, such as over voltage protection (OVP), brown-in/out protection, saturation protection, under voltage protection (UVP), over temperature protection (OTP), GND open protection and over current protection (OCP) with high / low line compensation. Therefore it can protect the system from damage due to occasional failure.

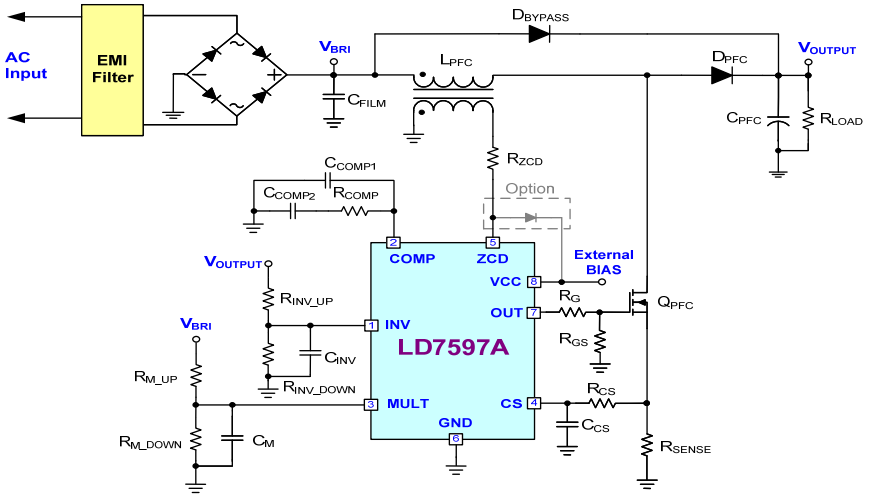
Features

- Critical conduction (CRM) or Discontinuous (DCM) Mode of PFC Pre-Regulator
- Peak Current Mode Control
- DCM operation with frequency limitation method
- Near-Unity Power Factor
- Ultra-Low THDi at Light Load Condition
- Line / Load Transient Enhance
- Brown-In/Out Detection on MULT pin
- ACOVP protection on MULT pin
- OVP (Output Overvoltage Protection) on INV pin
- UVP (Output Under-voltage Protection) on INV pin
- Saturation protection on CS pin
- GND open protection
- Internal OTP (Over Temperature Protection)
- 450/-850mA Driving Capability

Applications

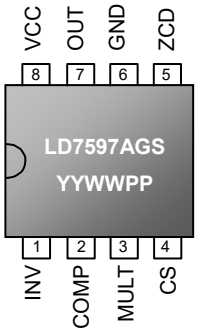
- Lighting Ballasts (LED, Fluorescent)
- All Off Line Appliances Requiring Power Factor Correction

Typical Application for Boost PFC



Pin Configuration

SOP-8 (TOP VIEW)



YY: Year code
WW: Week code
PP: Production code

Ordering Information

Part number	Package		Top Mark	Shipping
LD7597AGS	SOP-8	Green package	LD7597AGS	2500 /tape & reel

The LD7597AGS is RoHS compliant/ Green Packaged.

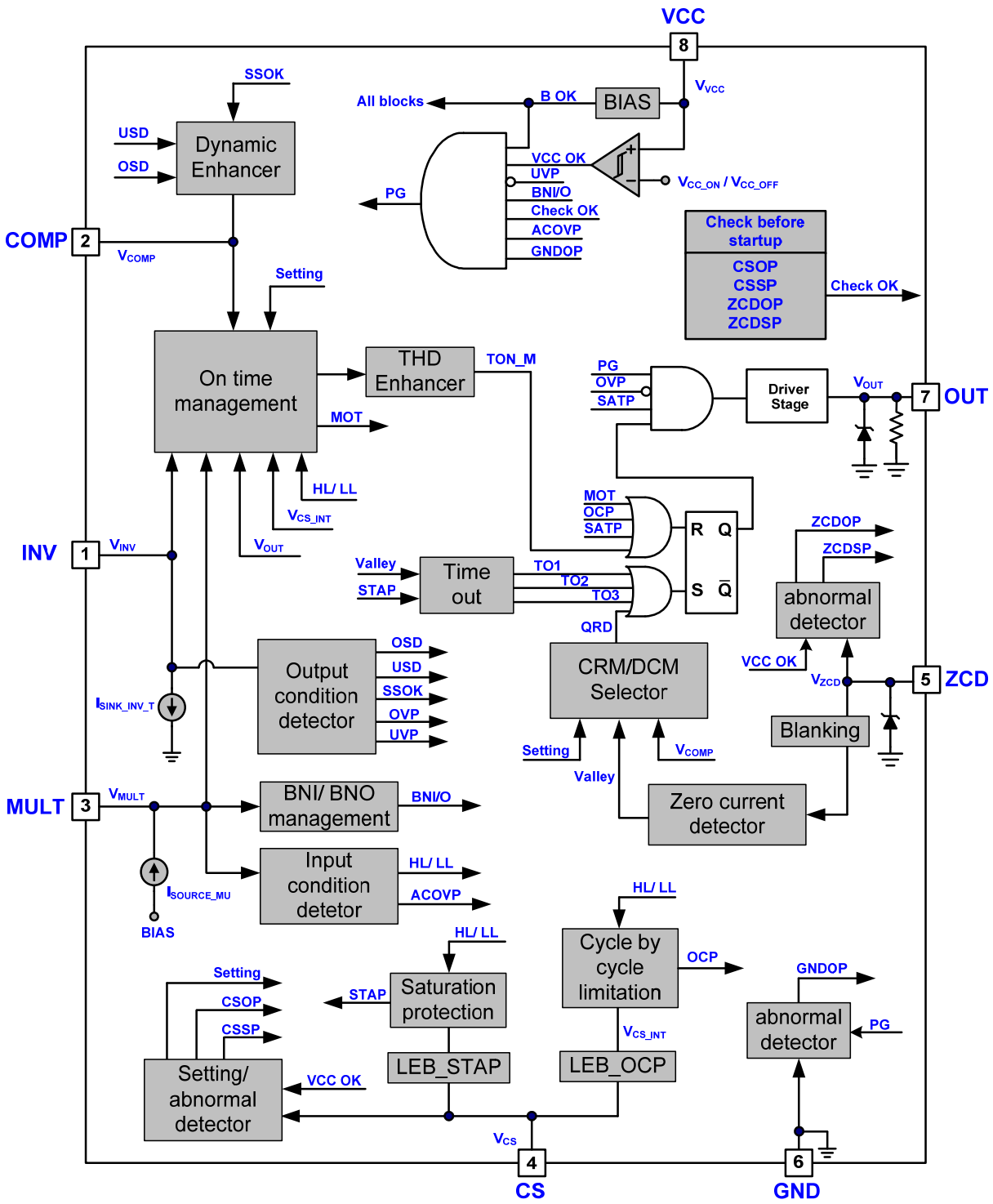
Protection Mode

Part number	UVLO(on)	UVLO(off)	BNO	SATP	ACOVP	OCP	GNDOP	Int. OTP
LD7597A	12.0V	7.5V	Auto	Auto	Auto	Cycle by Cycle	Auto	Auto

Pin Descriptions

Pin	Name	Function descriptions
1	INV	Output voltage feedback control. Built in output over voltage protection (OVP) and under voltage protection (UVP) function.
2	COMP	This pin is connected to the compensation network for power factor correction. The type II compensation is recommended
3	MULT	Multiplier input pin. Built in BNI/BNO and input overvoltage protection (ACOVP) function.
4	CS	This pin is used to monitor the current of MOSFET.
5	ZCD	This pin is used for zero current detection.
6	GND	Ground.
7	OUT	Gate drive output to drive the external MOSFET.
8	VCC	Supply voltage pin.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	-0.3V ~ 30V
OUT	-0.3V ~ VCC +0.3V
ZCD	-0.3V ~ 36V
ZCD source current	5mA
COMP, INV, MULT	-0.3V ~ 6.0V
CS	-0.3V ~ 6.0V
Maximum Junction Temperature	-40°C ~150°C(1)
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOP-8, θ_{JA})	160°C/W
Power Dissipation (SOP-8, at Ambient Temperature = 85°C)	250mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model	2.5 kV

Note1: For system application, refer to recommended operating conditions.

Caution:

Stress exceeding maximum ratings may damage the device. Maximum ratings are stress ratings only. Functional operation above the recommended operating conditions is not implied. Extended exposure to stress above recommended operating conditions may affect device reliability.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Junction Temperature	-40	125	°C
VCC Capacitance	22	100	μF
COMP Capacitance	0.1	4.7	μF
MULT pin Filter Capacitance	100	1000	pF
INV pin Filter Capacitance	0.1	22	nF
ZCD detection Resistor	30	100	kohm
ZCD source current		3	mA
CS pin Filter Capacitance		220	pF

Note：

1. Exceeding these ratings may damage the device.
2. When operation at harsh environment condition, as temperature and humidity or climate change …etc. Please pay attention to impedance variation between pin to pin or ground to avoid ripple remover closing loop and being failure.
3. The recommended operating conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Leadtrend does not recommend exceeding them or designing to absolute maximum ratings.
4. In selection of these external components, make sure that their values including temperature & tolerance characteristics are satisfied with the recommended ranges.

Electrical Characteristics

(VCC=14.0V, T_A = 25°C unless otherwise specified.)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
VCC Pin						
Startup current	V_{VCC} < V_{CC_ON}	I_{CC_ST}		1	3	μA
Operating current (with no load on OUT pin)	V_{COMP}=0V,no switching	I_{CC_OP1}		350	1500	μA
	*; 50kHz switching frequency condition	I_{CC_OP2}		2.5	3.0	mA
	V_{INV}=0V	I_{CC_OPA2}		65	120	μA
UVLO (off)		V_{CC_OFF}	7.0	7.5	8.0	V
UVLO (on)		V_{CC_ON}	11	12	13	V
Idle mode breaking time	*; Re-cycle time	T_{BRE}	40	60	80	ms
COMP Pin						
Transconductance amplifier		g_m	150	225	300	μmho
Maximum clamp voltage	*; V_{FB}=2V	V_{COMP_H}	4.27	4.50	4.73	V
Burst mode in threshold voltage		V_{BRI}	0.25	0.35	0.45	V
Maximum switching frequency	*	f_{SW_MAX}	340	400	460	kHz
Source current at USD is triggered during soft start	*; During soft start	I_{SOURCE_DS}	90	120	150	μA
Source current at USD is triggered after soft start	After soft start	I_{SOURCE_AS}	180	220	260	μA
Maximum on time limit by V_{COMP}	V_{COMP}=4.50V	T_{ON_MAX1}	26	30	36	μs
	*; V_{COMP}=0.55V	T_{ON_MAX2}	3.5	5.0	6.5	μs
INV Pin						
Internal reference voltage of error Amplifier	Tj=25 °C	V_{REF}	2.475	2.500	2.525	V
	Tj=-40~125 °C	V_{REF}	2.410	2.500	2.590	V
Undershoot detector (USD) threshold ratio	Percentage of V_{REF}	R_{USD}	90.0	92.0	93.5	%
Hysteresis of USD	*; Percentage of V_{REF}	$\triangle R_{USD_H}$	5.0	6.0	7.0	%
Overshoot detector (OSD) threshold ratio	Percentage of V_{REF}	R_{OSD}	105.5	107.0	108.5	%
Hysteresis of OSD	*; Percentage of V_{REF}	$\triangle R_{OSD_H}$	4	5	6	%
OVP threshold ratio	Percentage of V_{REF}	R_{OVP}	107.0	109.0	110.8	%
Hysteresis of OVP	*; Percentage of V_{REF}	R_{OVP_H}		R_{OSD}		%
UVP released threshold voltage	V_{INV} rising	V_{UVP_H}	0.40	0.45	0.50	V
UVP triggered threshold voltage	V_{INV} failing	V_{UVP_L}	0.15	0.20	0.25	V
Sink current of INV pin	*	$I_{SINK_INV_T}$	100	200	300	nA

(VCC=14.0V, T_A = 25°C unless otherwise specified.)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
MULT Pin						
Brown in (BNI) threshold voltage	assuming 1/Km=144	V_{BNI}	740	800	860	mV
De-bounce time of BNI	*, $V_{MULT} \geqq V_{BNI}$.	T_{DEB_BNI}		2	3	ms
Brown out (BNO) threshold voltage	assuming 1/Km=144	V_{BNO}	630	700	770	mV
De-bounce time of BNO	*	T_{DEB_BNO}	40	60	80	ms
High line detected threshold voltage	*	V_{HL}	1.51	1.65	1.79	V
Low line detected threshold voltage	*	V_{LL}	1.33	1.45	1.57	V
Source current of MULT pin	*	I_{SOURCE_MU}	100	200	300	nA
Gain of multiplier		KG_{MULT_HL}	0.08	0.09	0.10	1/V
		KG_{MULT_LL}	0.27	0.30	0.33	1/V
ACOVP threshold voltage		V_{ACOVP}	3.3	3.4	3.5	V
Hysteresis of ACOVP	*	V_{ACOVP_H}		-100		mV
ACOVP de-bounce time	*	T_{DEB_ACO}		150		µs
CS Pin						
Source current of CS pin before startup	Pulse width =160µs watchdog, before startup	I_{SOURCE_CS}	0.86	1.00	1.1	mA
CSSP threshold voltage	Before startup	V_{CSSP}	50	75	100	mV
CSOP threshold voltage	*; Before startup	V_{CSOP}	1.9	2.0	2.1	V
SATP threshold voltage	*; LL condition	V_{SATP_LL}	1.45	1.60	1.78	V
	*; HL condition	V_{SATP_HL}	0.75	0.85	0.95	V
Cycle by cycle limitation threshold		V_{OCP_HL}	0.54	0.60	0.66	V
	*	V_{OCP_LL}	0.95	1.05	1.15	V
LEB for cycle by cycle limitation	From OUT pin is rising.	T_{LEB_OCP}	280	350	420	ns
LEB for SATP	*; From OUT pin is rising.	T_{LEB_SATP}	80	150	220	ns

(VCC=14.0V, T_A = 25°C unless otherwise specified.)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
ZCD Pin						
Source current of ZCD pin before Startup	Pulse width =160μs watchdog before startup	I_{SOURCE_ZCD}	8.5	10.0	11.1	μA
ZCDOP threshold voltage	Before startup	V_{ZCDOP}	1.9	2.0	2.1	V
ZCDSP threshold voltage	Before startup	V_{ZCDSP}	120	175	235	mV
Zero current detection high threshold voltage	*; Rising	V_{QRDH}	0.675	0.750	0.825	V
Zero current detection triggered threshold voltage	*; Falling	V_{QRDL}	0.20	0.25	0.30	V
Time out for normal operating	*; $V_{ZCD} \geqq V_{QRDH}$ once during V_{OUT} is low and w/o V_{QRDL} signal.	TO1	30	35	40	μs
Time out for abnormal condition	$V_{ZCD} < V_{QRDH}$ during V_{OUT} is low.	TO2	150	200	250	μs
Time out for SATP	*; $V_{CS} \geqq V_{SATP_XL}$, From T_{LEB_SATP} to OUT pin is falling.	TO3	400	800	1200	μs
Blanking time for QRD	*; After gate-off.	T_{BLA}	0.5	1.0	1.5	μs
OUT Pin						
Output low level	*; VCC=12V, I_{SINK}=20mA	V_{OL}			0.5	V
Output high level	*; VCC=12V,I_{SOURCE}=20mA	V_{OH}		11.3		V
Output high clamp level	*; VCC=18V	V_{O_CLAMP}		13.5		V
Rising time	*; VCC=14V, CL=1nF	T_r		76		ns
Falling time	*;VCC=14V, C_L=1nF	T_f		26		ns
Internal OTP						
OTP trip level	*	T_{OTP}		140		°C
Hysteresis of OTP	*	ΔT_{OTP}		20		°C

*: Guaranteed by design.

Typical Performance Characteristics

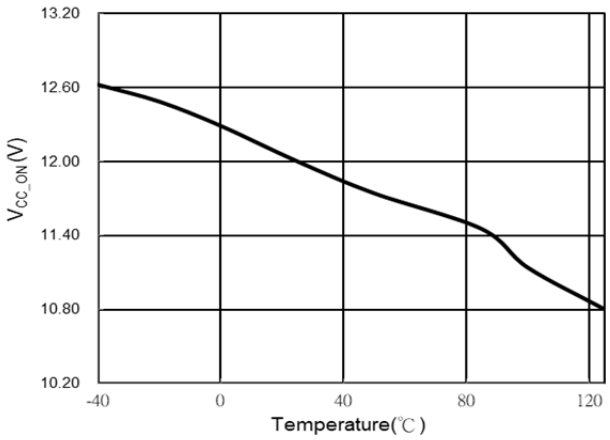


Fig.1 V_{CC_ON} VS. Temperature

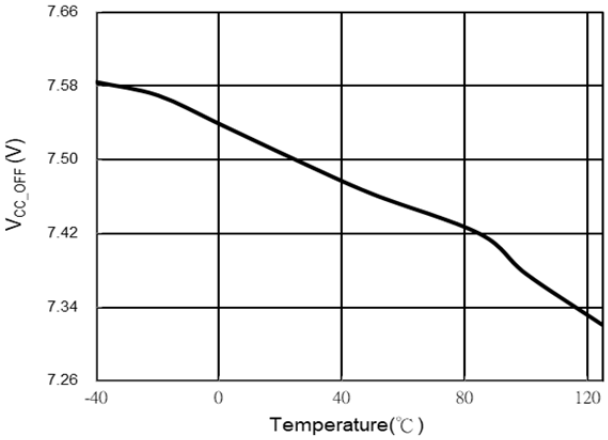


Fig.2 V_{CC_OFF} VS. Temperature

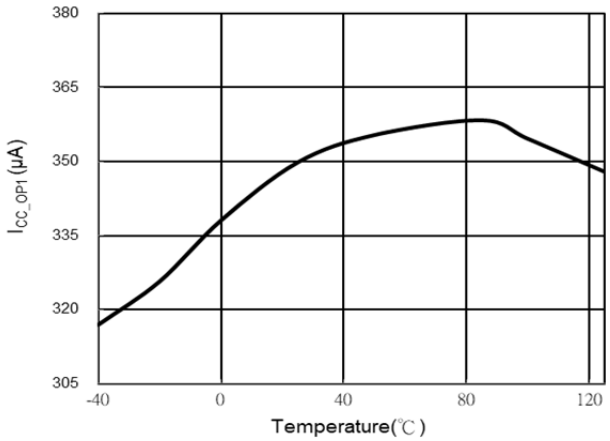


Fig.3 I_{CC_OP1} VS. Temperature

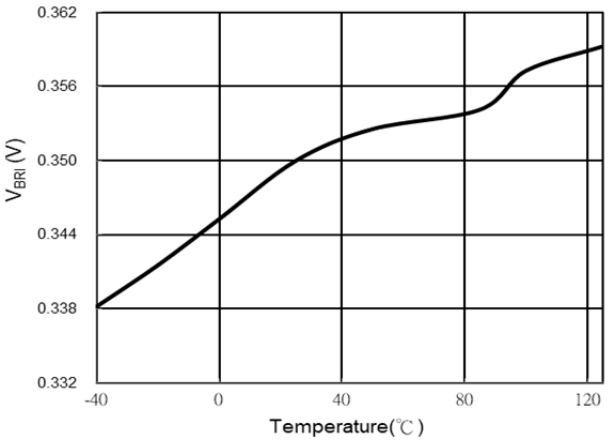


Fig.4 V_{BRI} VS. Temperature

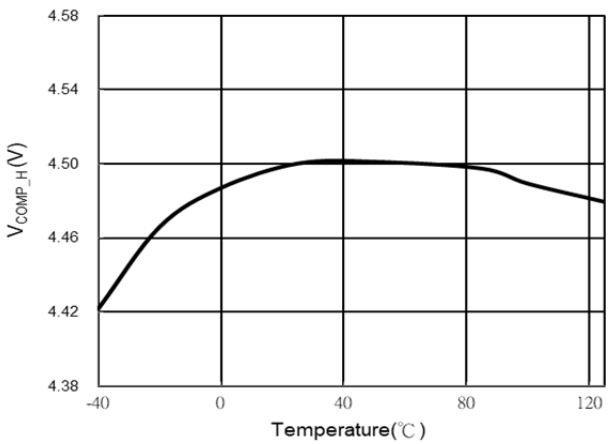


Fig.5 V_{COMP_H} VS. Temperature

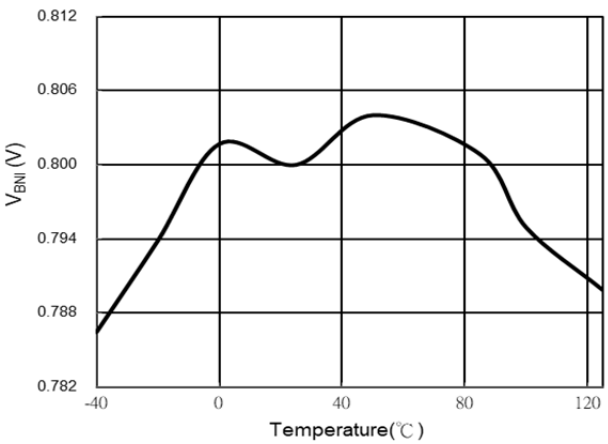


Fig.6 V_{BNI} VS. Temperature

Typical Performance Characteristics

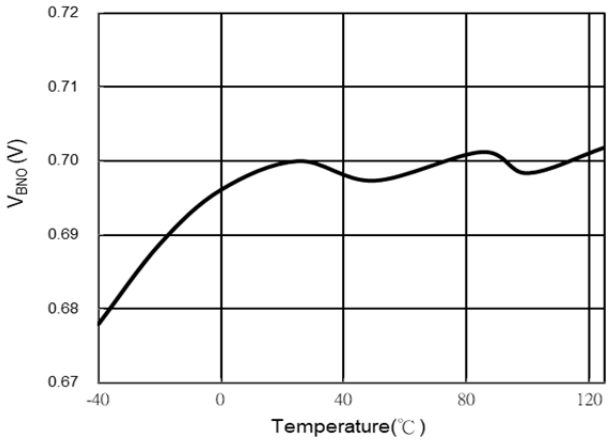


Fig.7 V_{BNO} VS. Temperature

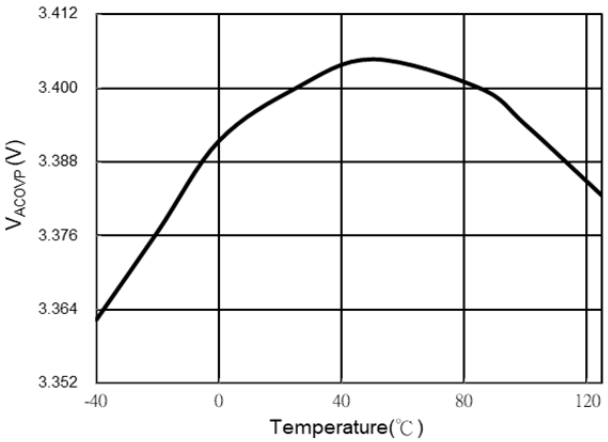


Fig.8 V_{ACOVP} VS. Temperature

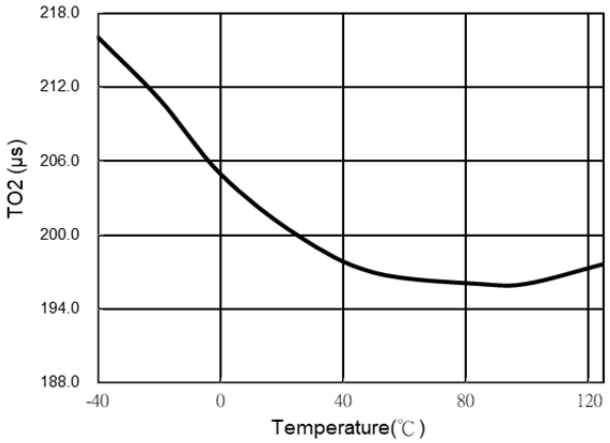


Fig.9 TO2 VS. Temperature

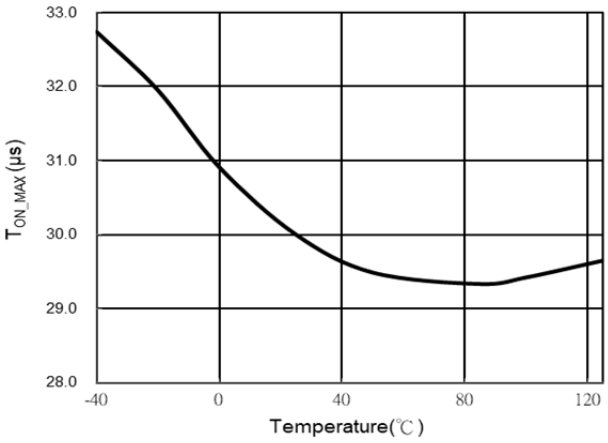


Fig.10 T_{ON_MAX} VS. Temperature

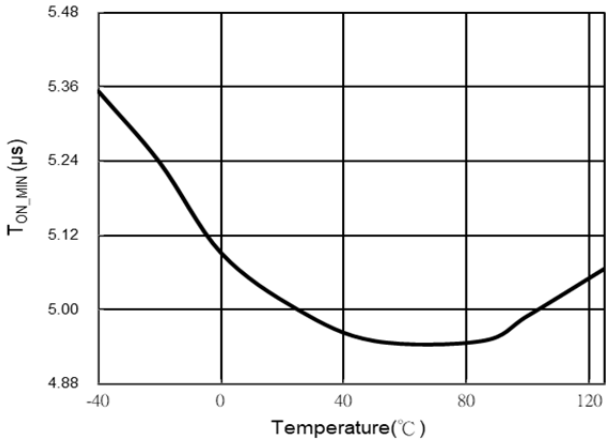


Fig.11 T_{ON_MIN} VS. Temperature

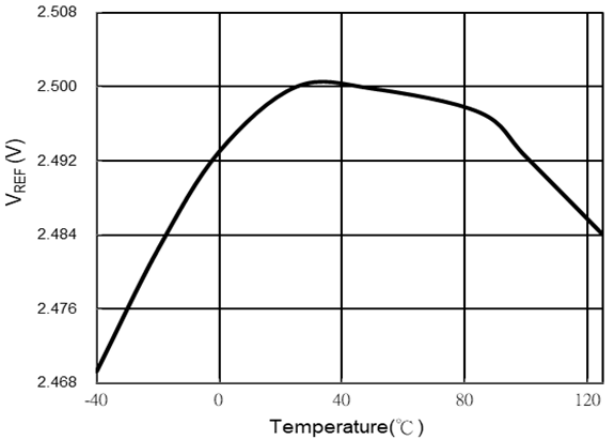


Fig.12 V_{REF} VS. Temperature

Typical Performance Characteristics

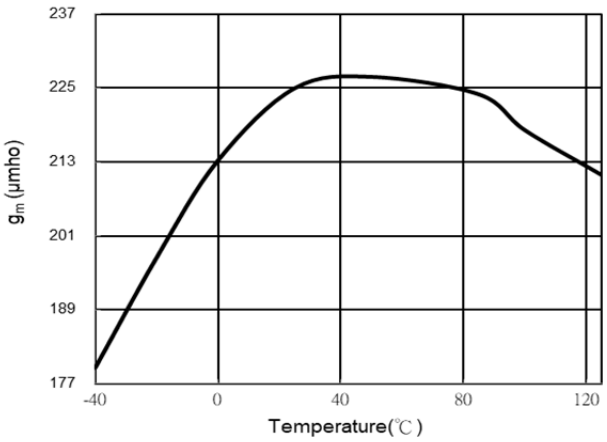


Fig.13 g_m VS. Temperature

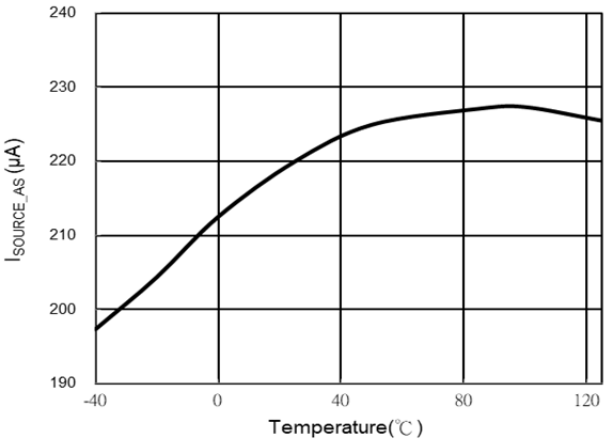


Fig.14 I_{SOURCE_AS} VS. Temperature

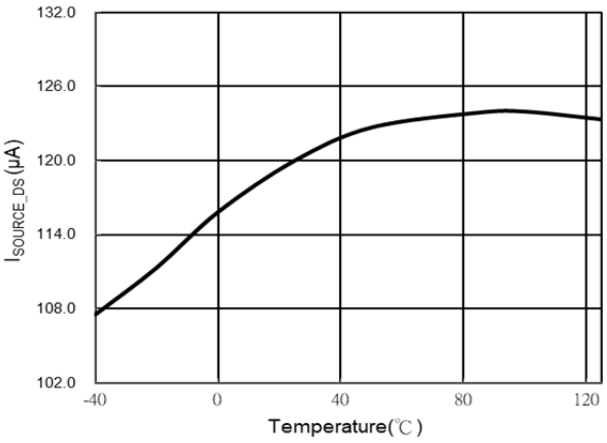


Fig.15 I_{SOURCE_DS} VS. Temperature

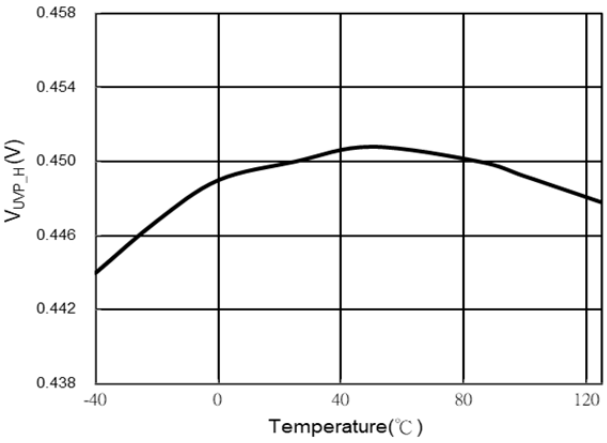


Fig.16 V_{UVP_H} VS. Temperature

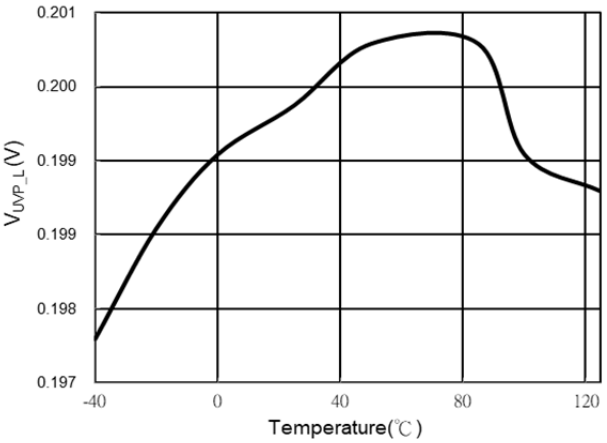


Fig.17 V_{UVP_L} VS. Temperature

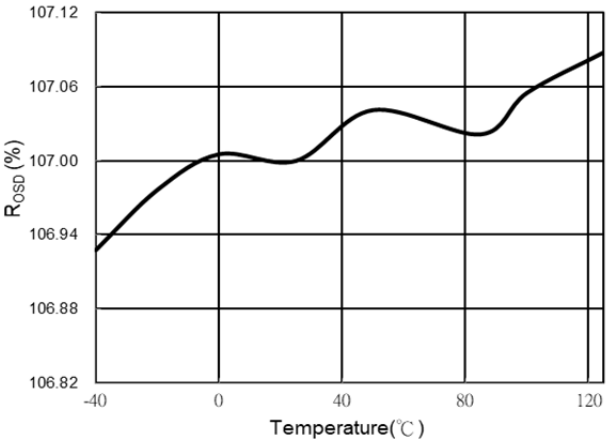


Fig.18 R_{OSD} VS. Temperature

Typical Performance Characteristics

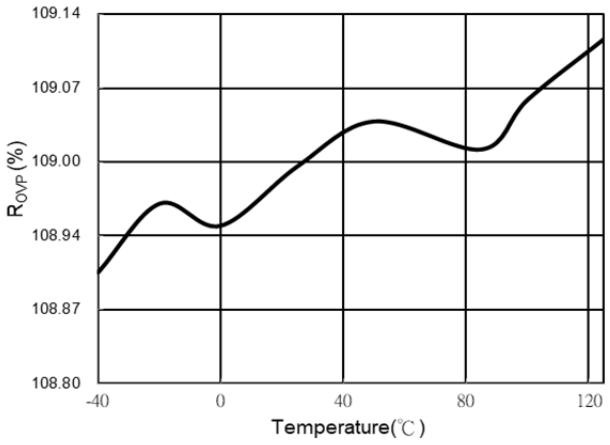


Fig.19 R_{OVP} VS. Temperature

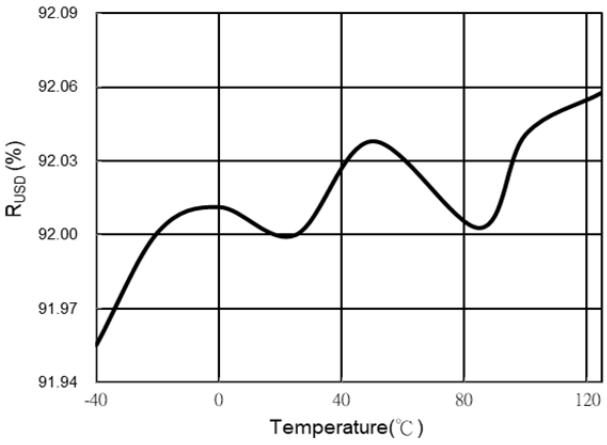


Fig.20 R_{USD} VS. Temperature

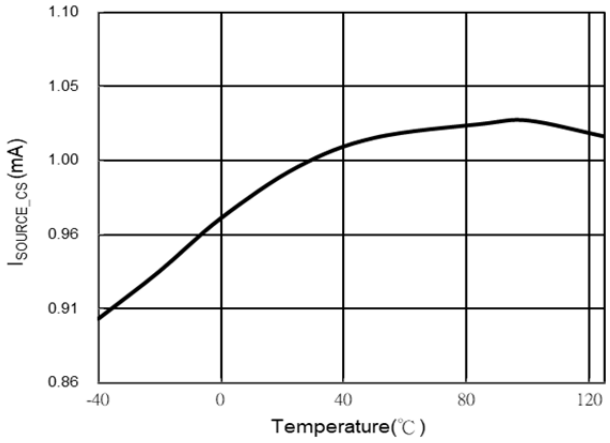


Fig.21 I_{SOURCE_CS} VS. Temperature

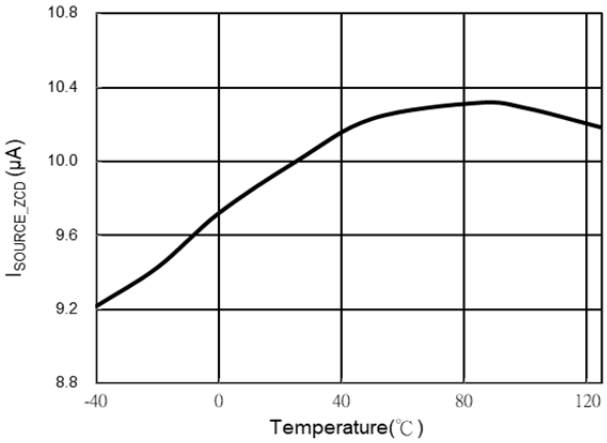


Fig.22 I_{SOURCE_ZCD} VS. Temperature

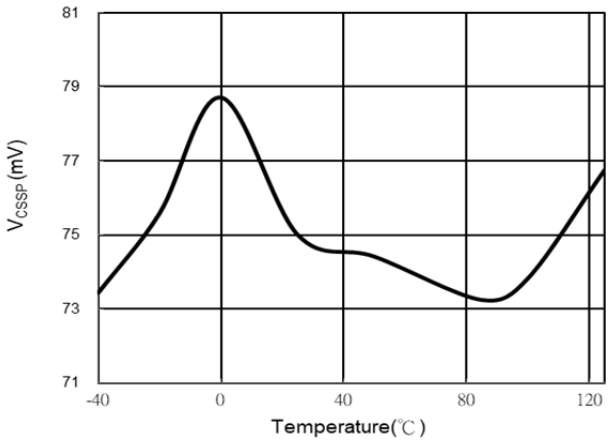


Fig.23 V_{CSSP} VS. Temperature

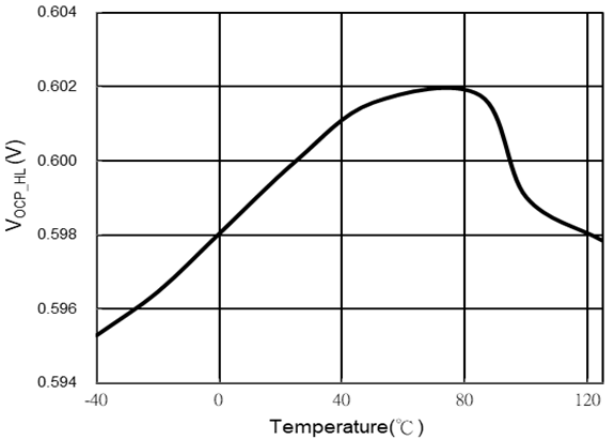


Fig.24 V_{OCP_HL} VS. Temperature

Typical Performance Characteristics

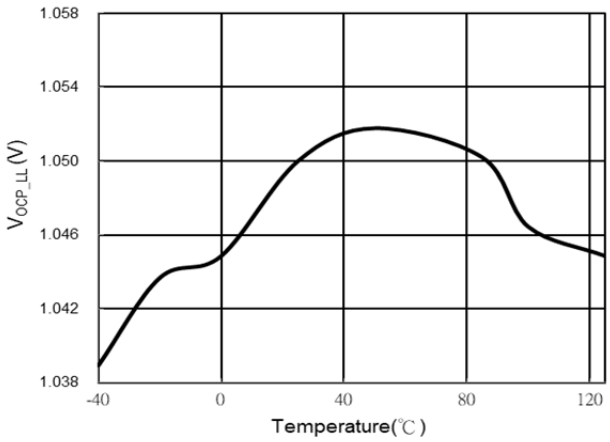


Fig.25 V_{OCP_LL} VS. Temperature

Application Information

Operation Overview

LD7597A is designed for power factor correction with boost topology. It's achieved the high efficiency across the all operating range of line and load with DCM operation and frequency limitation method. Base on the current mode control algorithm with THD improved function, LDA could operate as transition mode at full load condition or DCM mode at light load condition with ultra-low THD.

Zero Current Detection (ZCD)

The block of zero current detection will detect auxiliary winding signal to drive MOSFET. As shown in Fig.26. During gate off, if V_{ZCD} is higher than V_{QRDH} (0.75V, typ. Level trigger once) then each time lower under V_{QRDL} (0.25V, typ. falling edge trigger) as valley signal, the current of inductor will be closed zero at first valley. According to V_{COMP} level, valley signal will be selected and became QRD signal to turn on MOSFET again. For typical application (output=390~450V), Recommended the turn ratio of transformer is around 10.

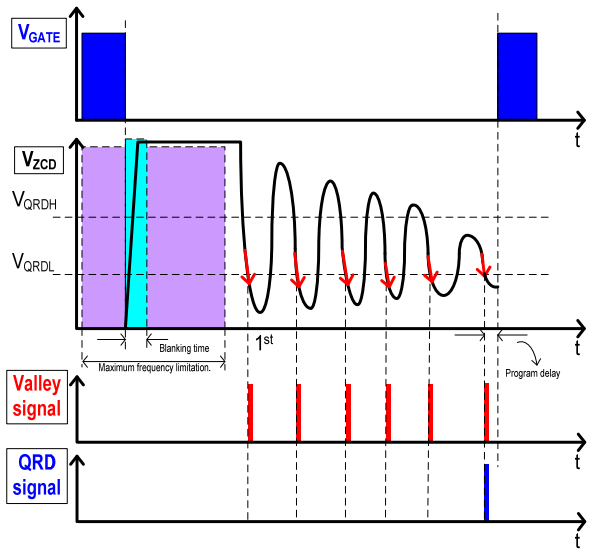


Fig.26

ZCD check after VCCOK

As shown in Fig.27. After VCCOK ($V_{VCC} \geqq V_{CC_ON}$, 12.0V, typ.), LD7597A provides an internal constant current source (I_{SOURCE_ZCD}, 10μA, typ.) for ZCD pin about 160μs (T_{CHECK}, typ.). V_{ZCD} is detected to check the condition of soldered. If V_{ZCD} is higher than V_{ZCDOP} (2.0V, typ.), ZCDOP is triggered. LD7597A operates into idle mode and re-check again after T_{BRE} (60ms, typ.). If V_{ZCD} is lower than V_{ZCDSP} (175mV, typ.), ZCDSP is triggered. LD7597A operates into idle mode and re-check again after T_{BRE}. Once $V_{ZCDSP}<V_{ZCD}<V_{ZCDOP}$, ZCD check is pass and LD7597A is ready to operates into next stage.

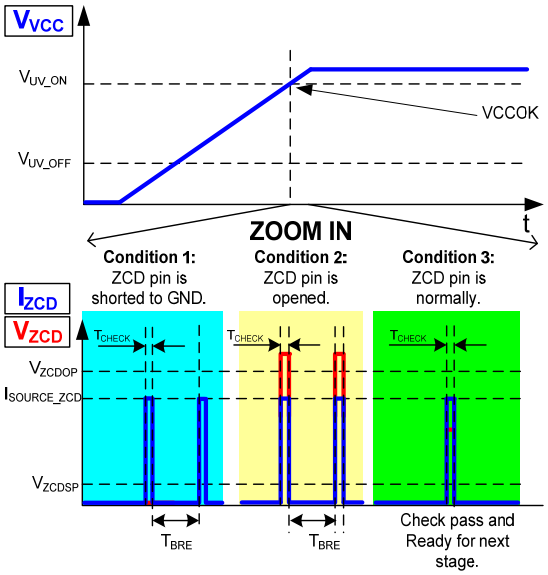


Fig.27

Time Out function

During gate off time, if valley signal is triggered but without QRD signal, the time-out 1 function is active. The switching period is limited at TO1 (35μs, typ.). As shown in Fig.28. The other condition, during off time, if valley signal is not triggered, the time-out 2 function is active. The switching period is limited at TO2 (200μs, typ.). As shown in Fig.29.

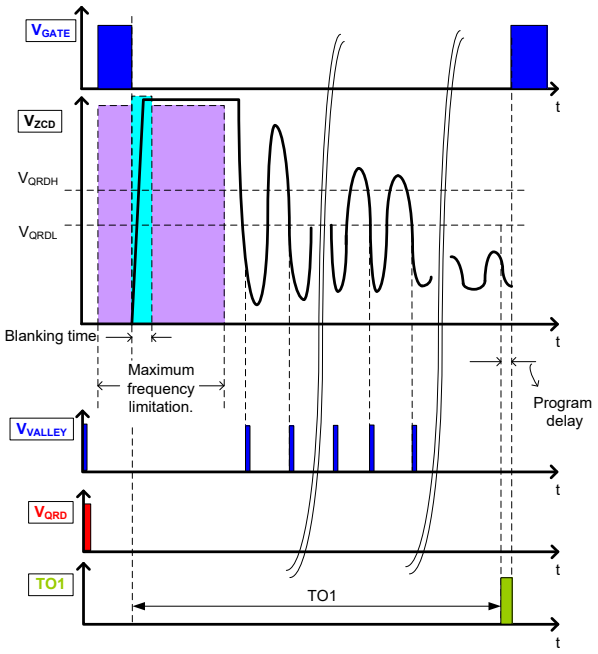


Fig.28

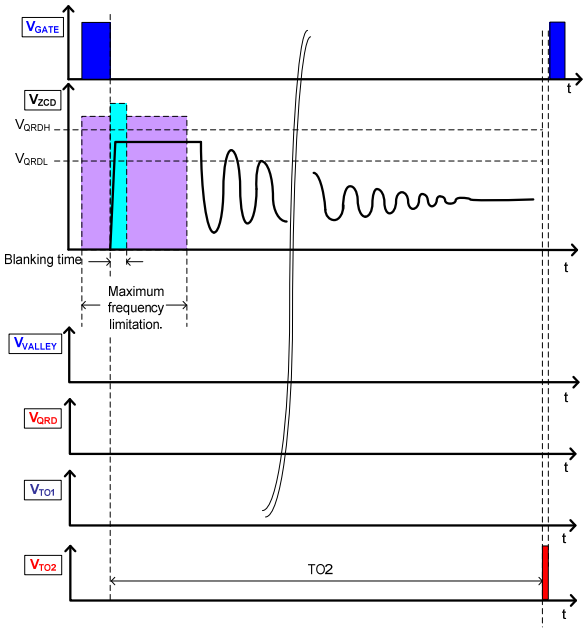


Fig.29

When OUT pin is rising and after T_{LEB_SATP}, once V_{CS} is higher than V_{SATP_XL} (1.6V at HL, 0.85 at LL). OUT pin is off immediately and TO3 function (Saturation protection, STAP) is active, the switching period is limited at TO3 (800μs, typ.) to prevent any damaged. As shown in Fig.30.

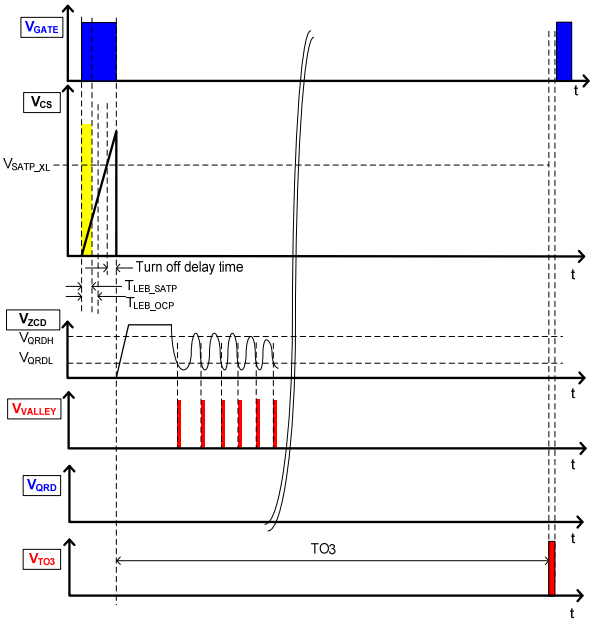


Fig.30

Current Sense

CS setting and Check before startup

After VCCOK, LD7597A provides an internal constant current source (I_{SOURCE_CS}, 1mA, typ.) for CS pin about 160μs (T_{CHECK}, typ.), this V_{CS} is detected to set operation at transition mode or DCM mode of V_{COMP} threshold level and check the condition of soldered. If V_{CS} setting voltage is lower than V_{CSSP} (75mV, typ.) CSSP is triggered. LD7597A operates into idle mode and re-setting again after T_{BRE}. If V_{CS} is higher than V_{CSOP} (2.0V, typ.), CSOP is triggered. V_{CS} is always pulled high until fault condition is removed and LD7597A recheck CS pin condition again. If $V_{CSSP}<V_{CS}<V_{CSOP}$, CS check is pass and LD7597A is ready to operates into next stage. As shown in Fig.31.

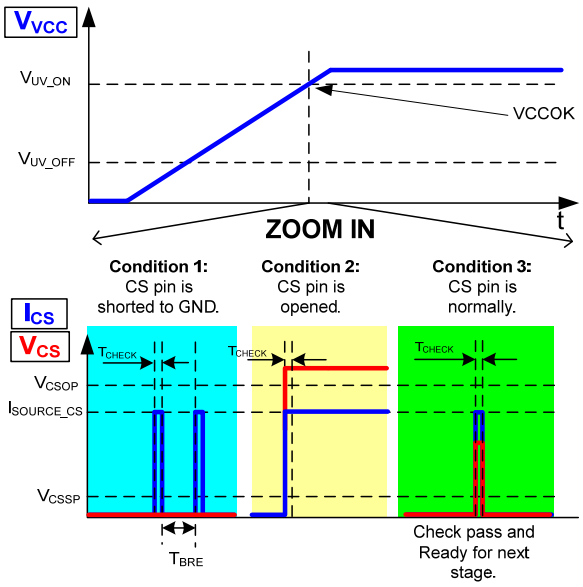


Fig.31

Current Mode Control and THD Compensation

LD7597A is current mode control PFC controller. Different to traditional current mode PFC controller is the error amplifier. It uses the transconductance amplifier to replace the operational amplifier. That will increase the operable range of COMP pin and suit for LED application. As shown in Fig.32. For DCM operation, LD7597A built in the internal compensation circuit to modify on time to achieve the high PF and low THD.

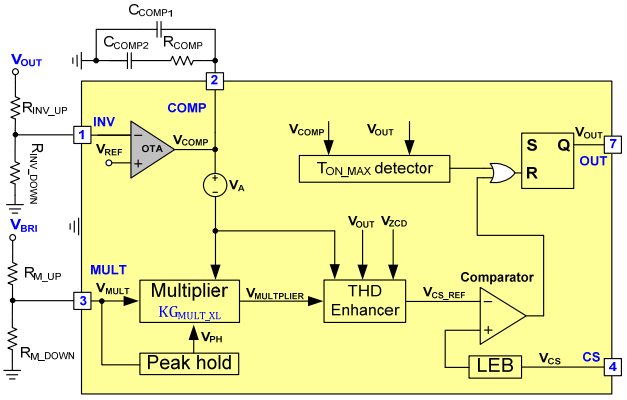


Fig.32

According to the function block and ignore the THD enhancer, obtained the following equations,

$$V_{CS_REF} \approx V_{MULTIPLIER} \approx V_{MULT} \times (V_{COMP} - V_A) \times KG_{MULT_XL} \quad \text{(eq.1)}$$

Where: KG_{MULT_XL} is gain of multiplier, if low line input K_{GMULT_LL}=0.3 (typ.), if high line input K_{GMULT_HL}=0.09 (typ.). V_A=0.5V (typ.).

Due to the THD improved function, LD7597A is operating at VOT (Variable On-time) method. As shown in fig.33.

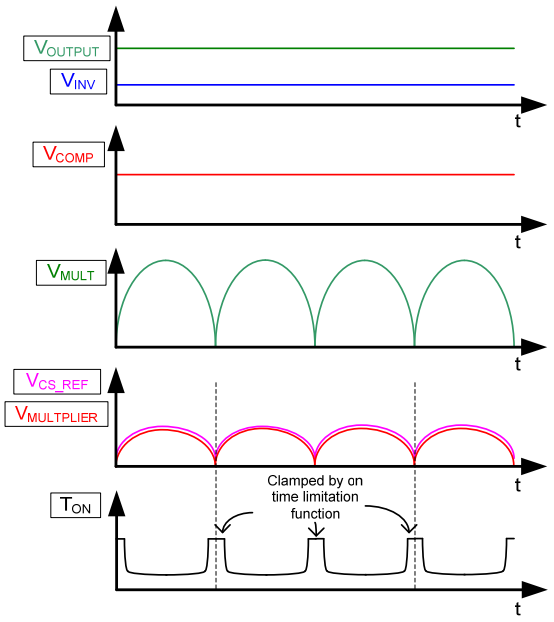


Fig.33

The output voltage is defined as below.

$$V_{OUTPUT} = V_{REF} \times \frac{R_{INV_DOWN} + R_{INV_UP}}{R_{INV_DOWN}} \quad \text{(eq.2)}$$

Where V_{REF}=2.5V (typ.).

Recommended resistance of R_{INV_DOWN} range is 20k~33k ohm.

On Time Limitation

Due to LD7597A operates at VOT method and it turns on the MOSFET almost 100 percent duty cycle near the zero crossing of input AC voltage. That will cause the current distortion by spike. So add another on time limitation function is necessary which is controlled by V_{COMP}, obtained the following equations,

$$T_{ON_MAX} = \left(6.311\frac{\mu s}{V} \times V_{COMP}\right) + 1.6\mu s \quad \text{(eq.3)}$$

From the equation 3, the maximum on time is 30μs (typ.) at V_{COMP} equals to 4.5V. The maximum on time is 5.0μs (typ.) at V_{COMP} equals to 0.55V.

Transconductance Amplifier

As shown in Fig.34. Gain of OTA is 225μmho (typ.) at the range of V_{INV} is from V_{REF}-0.1V (typ.) to V_{REF}+0.1V (typ.). The maximum sink (I_{SINK_MAX}) and source (I_{SOURCE_MAX}) current is 22.5μA (typ.). The non-inverting input terminal of OTA is connected to the reference voltage (V_{REF}, 2.5V, typ.).

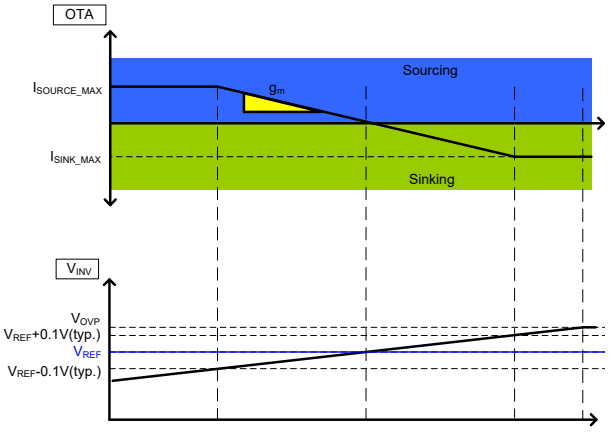


Fig.34

Function of MULT Pin

Source current for MULT pin open status

LD7597A provides an internal constant source current (I_{SOURCE_MU}) about 200nA (typ.) for MULT pin open protection. Once it is open, MULT pin is pulled high immediately. ACOVP is triggered after de-bounce time and auto-recovery when the fault condition is removed.

Brown in/ out and high/ low line detected function

LD7597A implements the peak voltage holding function on MULT pin. The peak voltage of MULT pin (V_{PH}) is used for high/low line detection. The voltage of MULT pin (V_{MULT}) is used for brown in/out. As shown in Fig.35.

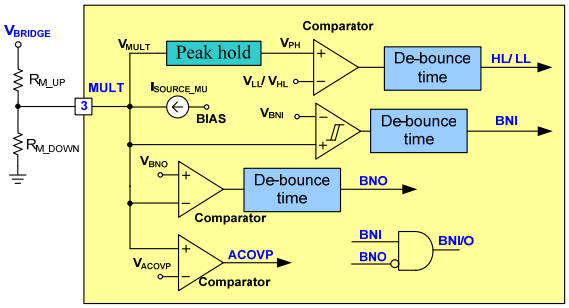


Fig.35

BNO/BNI function

As shown in Fig.36. If V_{MULT} is higher than V_{BNI} (800mV, typ.) with de-bounce time T_{DEB_BNI} (3ms, max.), the BNI is triggered and if others check (ZCD, CS, UVP check) are pass, LD7597A operates into next stage and gate begin switching. If V_{MULT} is lower than V_{BNO} (700mV, typ.) with de-bounce time T_{DEB_BNO} (60ms, typ.), the on time will decreased smoothly until zero on time to avoid the false triggered of BNI again.

HL/LL detect function

The HL/LL condition is defined by V_{PH}. If V_{PH} is higher than V_{HL} (1.65V, typ.) with de-bounce time 1ms (max.), the HL condition is triggered and LD7597A changes the key parameters for high line input. Once V_{PH} is lower than V_{LL} (1.45V, typ.) with de-bounce time 25ms (typ.), the LL condition is triggered and LD7597A changes the key parameters for low line input.

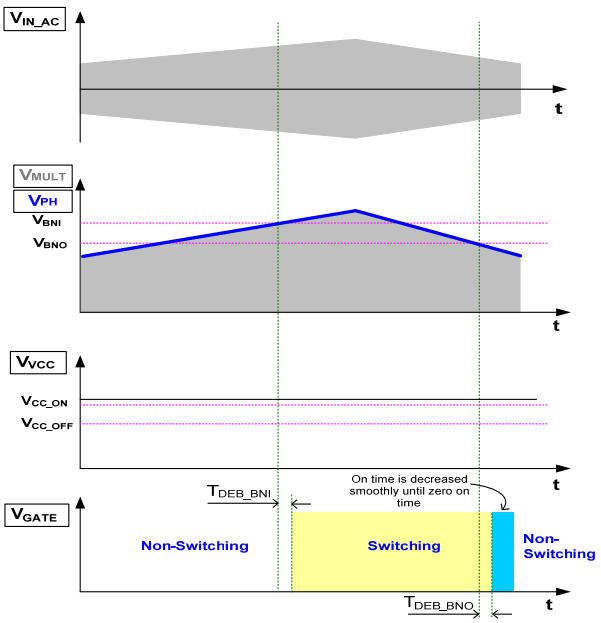


Fig.36

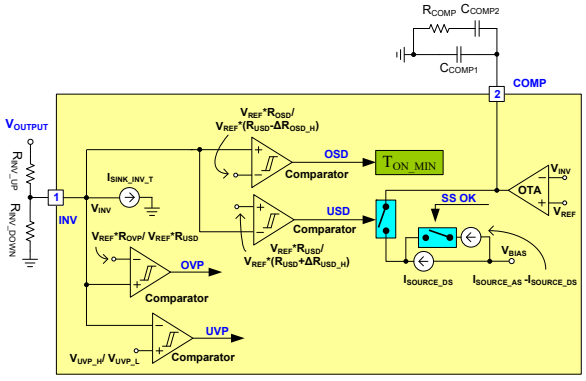


Fig.37

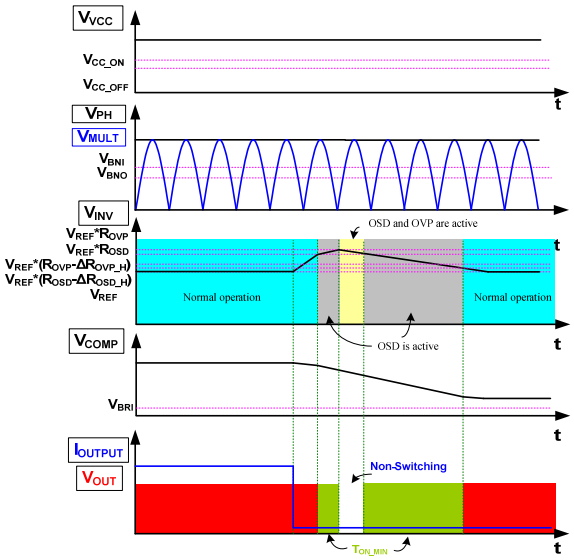


Fig.38

Dynamic Improved and OVP of INV Pin

Sink current for INV pin open status

Internal constant current source ($I_{SINK_INV_T}$) always provides about 200nA (typ.) for INV pin open protection. Once it is open, INV pin is pulled low to ground immediately. UVP is triggered and LD7597A operates into idle mode.

Dynamic improved (Overshoot detector, OSD)

As shown in Fig.37 and Fig.38. The inverting input of OSD comparator is connected to V_{REF_OSD} (R_{OSD}*V_{REF}), if V_{INV} is higher than V_{REF_OSD}, OSD is triggered, T_{ON} is minimum to limit output voltage rising until the V_{INV} is lower than ((R_{OSD}-△R_{OSD_H})* V_{REF}).

Dynamic improved (Undershoot detector, USD)

The non-inverting input of USD comparator is connected to V_{REF_USD} (R_{USD}*V_{REF}). During soft start, once USD is triggered, I_{SOUCRE_DS} (120μA, typ.) is active to pull V_{COMP} high until the V_{INV} is lower than ((R_{USD}+△R_{USD_H})* V_{REF}). After soft start (V_{INV}> V_{REF_USD}), I_{SOUCRE_AS} (220μA, typ.) is active and waiting to the next USD is occurred. As shown in Fig.39.

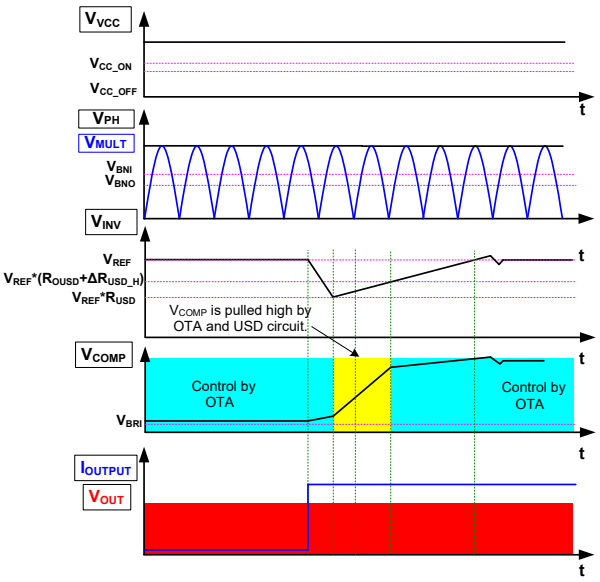


Fig.39

Over voltage protection

As shown in Fig.40. If V_{INV} is higher than V_{OVP} (R_{OVP}*V_{REF}), OVP is triggered. LD7597A is gate off immediately until V_{INV} is lower than (R_{OSD}* V_{REF}). During OVP is triggered, V_{COMP} is pulled low by OTA circuit.

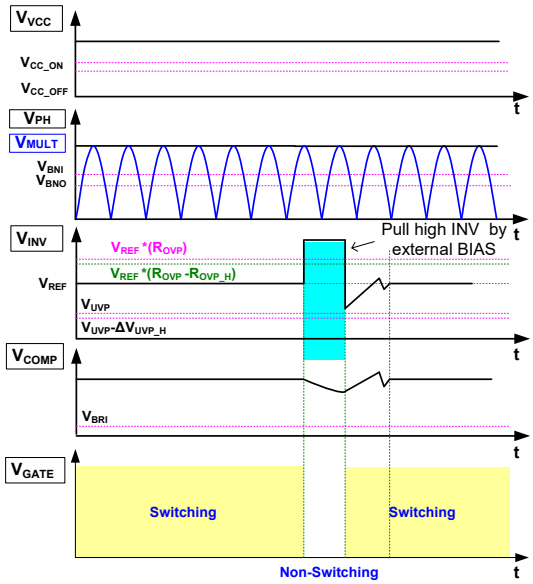


Fig.40

Under voltage protection

As shown in Fig.41. After VCCOK, if V_{INV} is lower than V_{UVP_L} (0.2V, typ.), UVP is triggered, LD7597A is gate off immediately until V_{INV} is higher than V_{UVP_H} (0.45V, typ.).

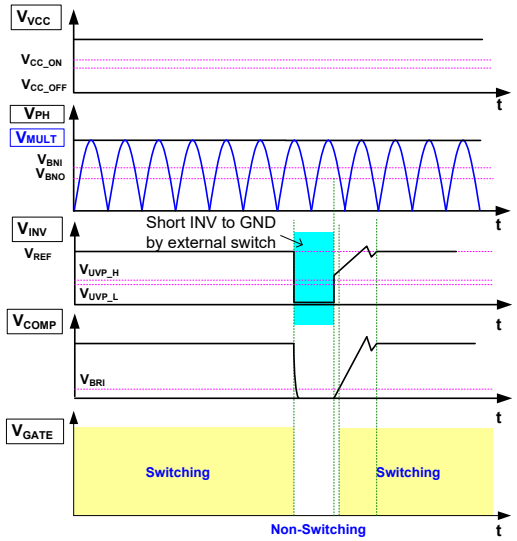


Fig.41

Over current protection

LD7597A provides the cycle by cycle current limitation by monitor CS pin. After T_{LEB_OCP} (350ns, typ.), if V_{CS} is higher than V_{OCP_XL}, OCP is triggered. The gate is off immediately until next switching cycle. V_{OCP_XL} is defined as table.1.

	LL condition	HL condition
V_{OCP_XL}	1.05V (typ.)	0.6V (typ.)

Table.1

AC over voltage protection

If $V_{MULT} \geqq V_{ACOVP}$ with de-bounce time T_{DEB_ACO} (150μs, typ.), ACOVP is detected, LD7597A will gate off immediately to prevent from any damage until the internal signal V_{MULT} is lower than V_{ACOVP} -V_{ACOVP_H}. As shown in Fig.42.

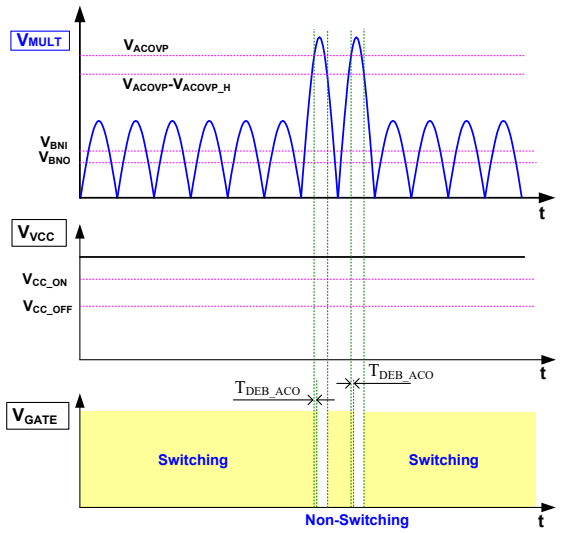


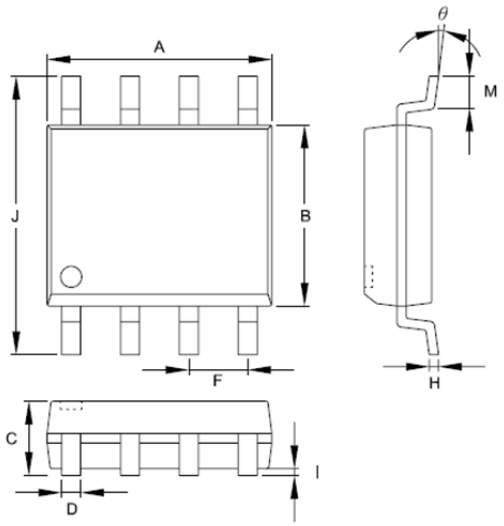
Fig.42

Internal Over Temperature Protection (int. OTP)

When the junction temperature reaches 140°C approximately, the thermal sensor signals would stop IC's switching. If the IC's junction temperature cools by 20°C or VCC restart again.

Package Information

SOP-8



Symbol	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Revision History

REV.	Date	Change Notice
00	07/10/2023	Original Specification.

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice.

Customers should verify the datasheets are current and complete before placing order.