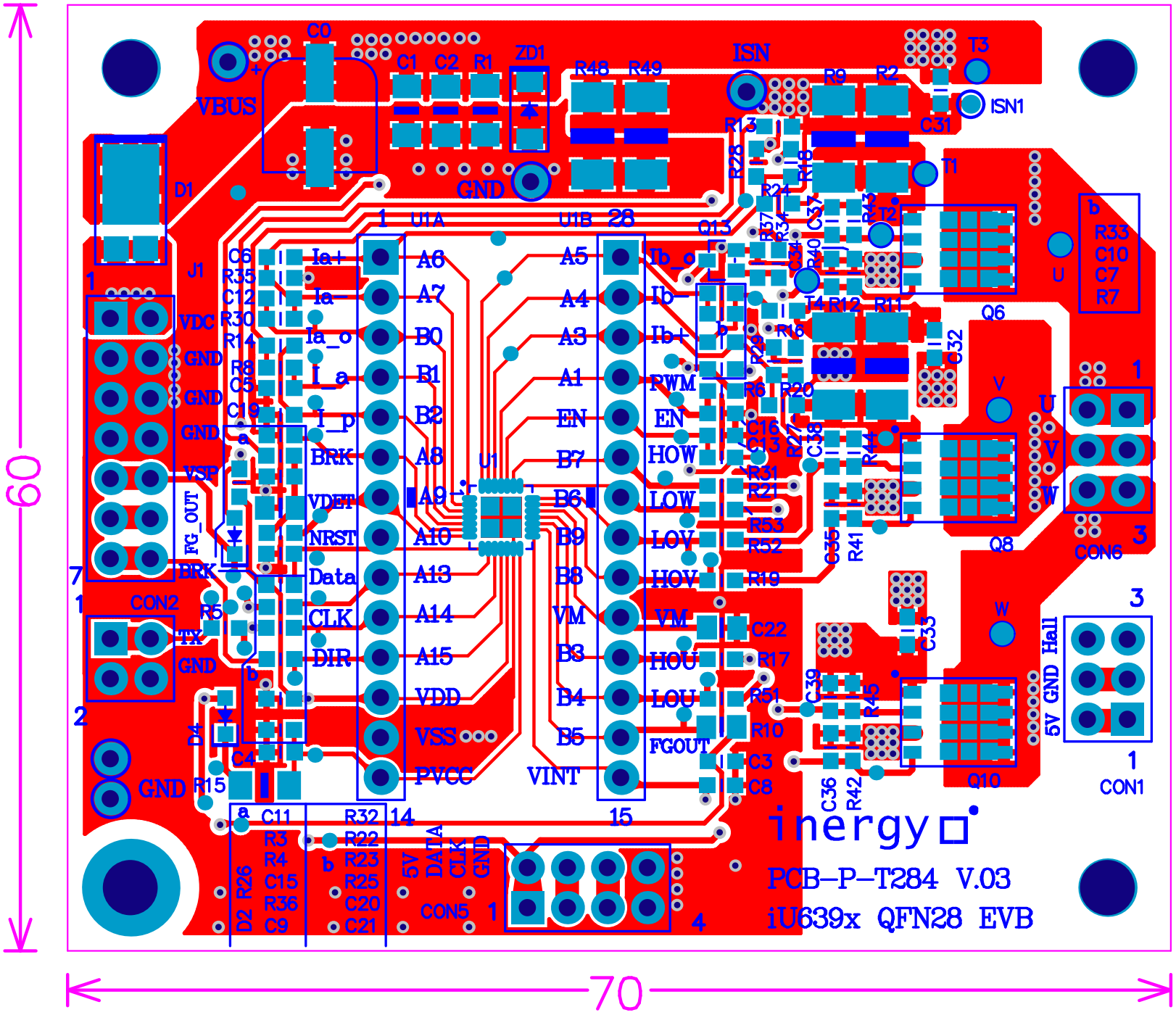
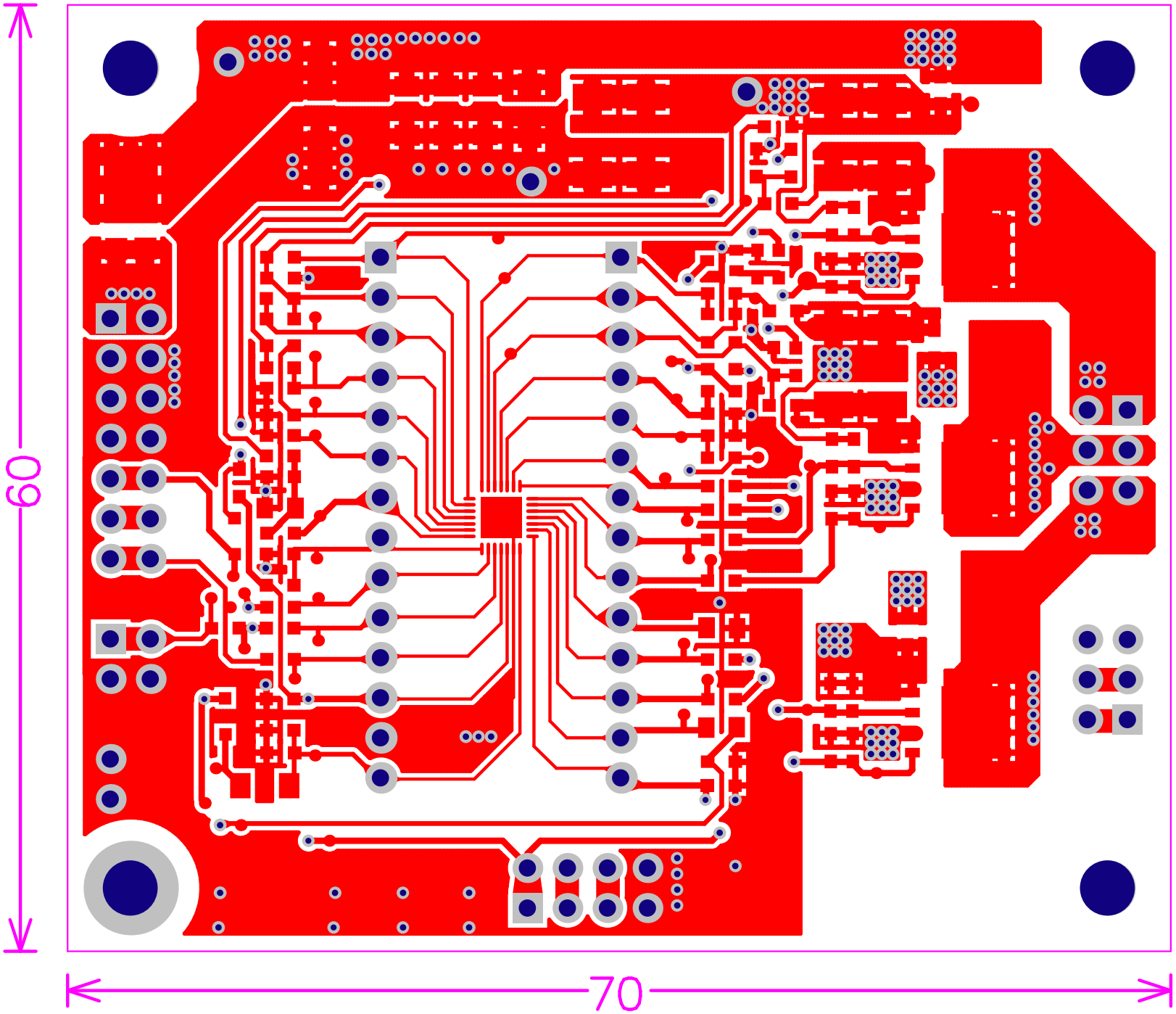
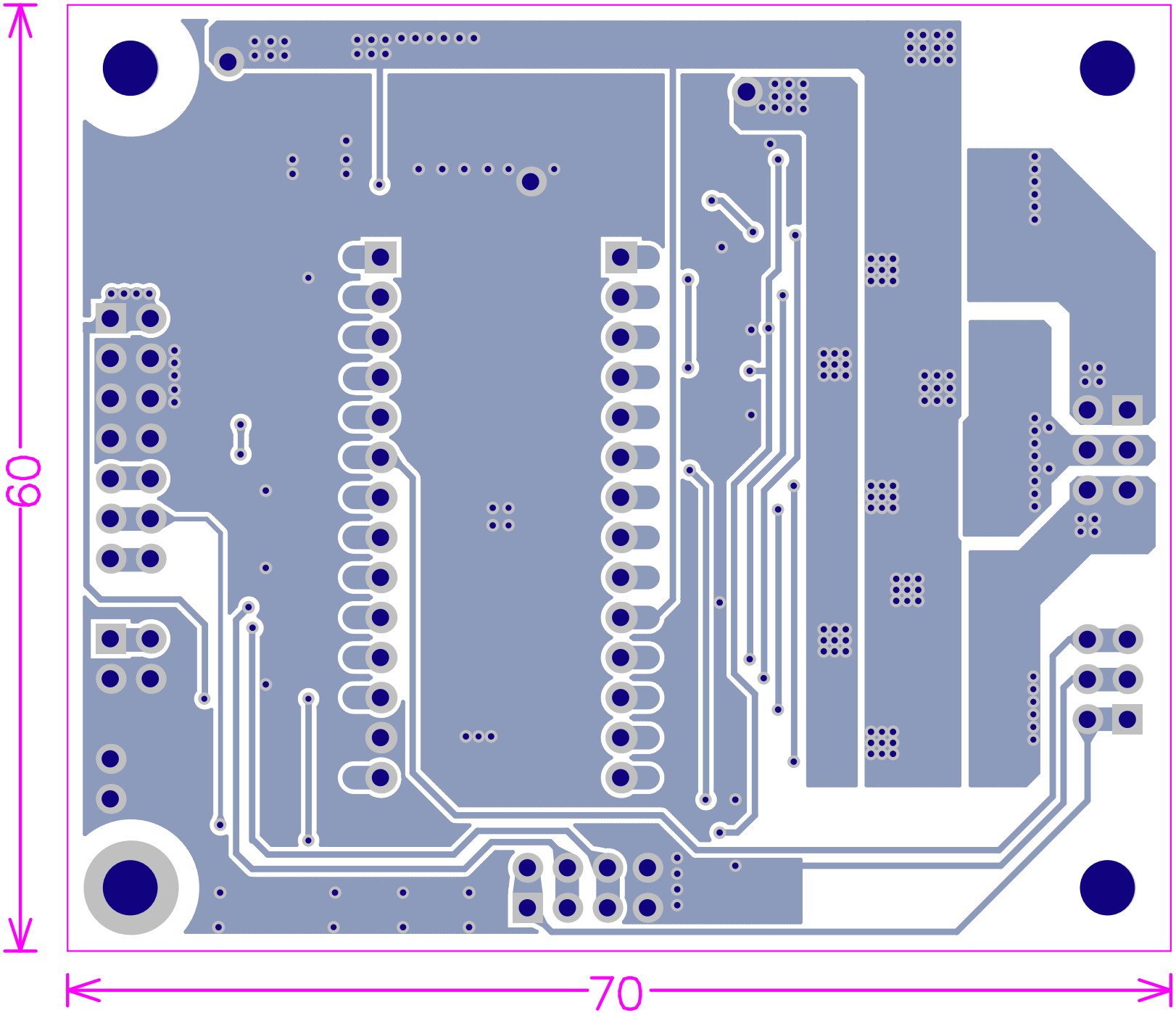

60
70
VBUS
GND
ISN
ISN1
T1
T2
T3
T4
U
V
W
J1
VDC
GND
VSP
BRK
FG_OUT
CON2
TX
GND
CON1
Hall
5V
GND
CON5
CON6
U1A
U1B
U1
Ia+
Ia-
Ia_o
I_a
I_p
BRK
VDET
NRST
Data
CLK
DIR
VDD
VSS
PVCC
A6
A7
B0
B1
B2
A8
A9
A10
A13
A14
A15
A5
A4
A3
A1
EN
B7
B6
B9
B8
VM
B3
B4
B5
VINT
Ib_o
Ib-
Ib+
PWM
EN
HOW
LOW
LOV
HOV
VM
HOU
LOU
FGOUT
DATA
CLK
GND
Q6
Q8
Q10
Q13
inergy
PCB-P-T284 V.03
iU639x QFN28 EVB
TOP Layer + Overlay color

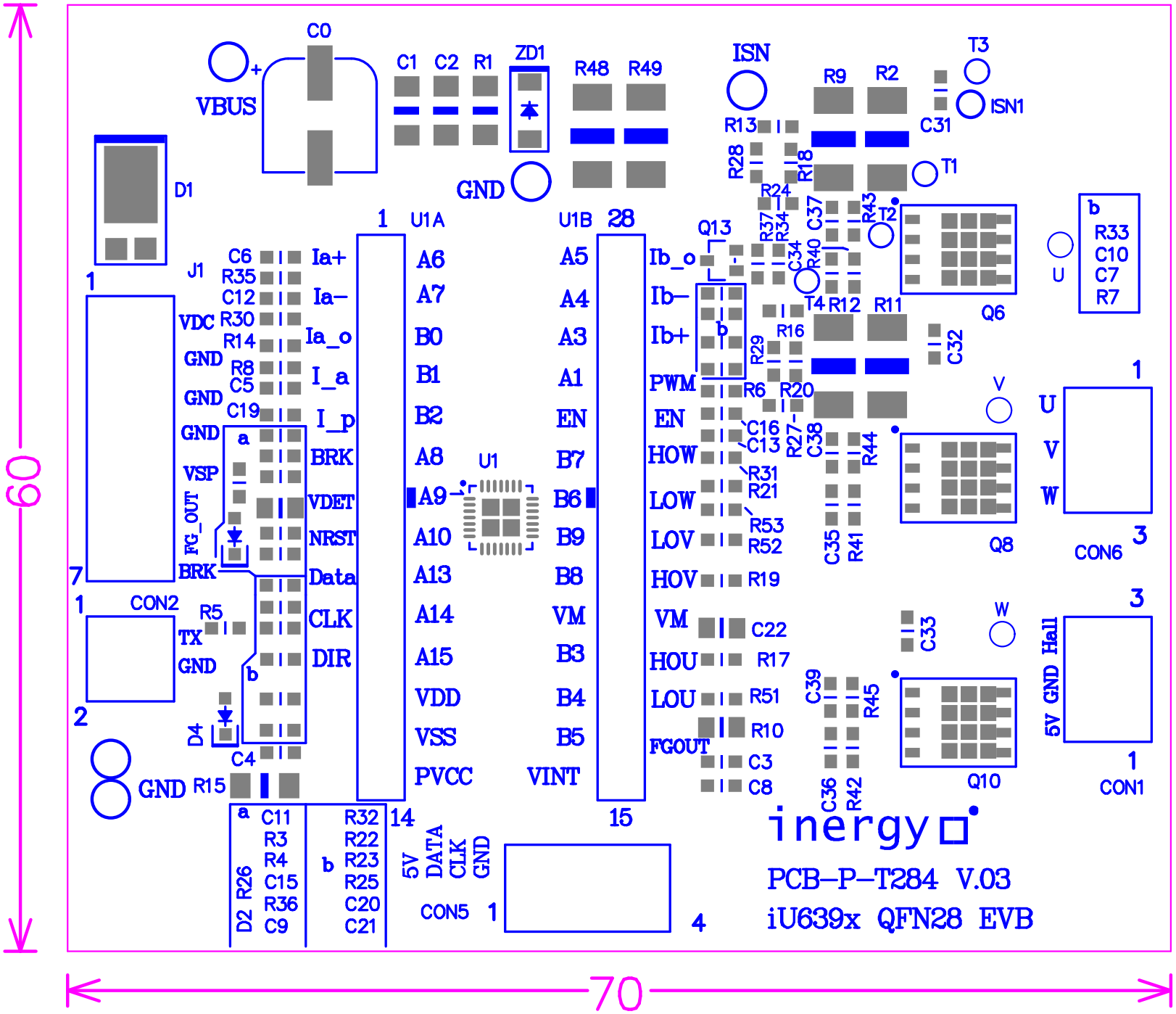
BOTTOM Layer + Overlay color



Top Layer



Bottom Layer


C0
VBUS
C1
C2
R1
ZD1
R48
R49
GND
ISN
R9
R2
T3
ISN1
C31
R13
R28
R18
T1
R24
R37
R34
C37
R43
T2
C34
R40
T4
R12
R11
Q6
R16
C32
R29
R6
R20
V
C16
C13
R27
C38
R44
R31
R21
R53
R52
R19
C35
R41
Q8
C22
R17
R51
R10
C3
C8
C33
W
C39
R45
C36
R42
Q10
U1
U1A
U1B
1
28
15
14
A6
A7
B0
B1
B2
A8
A9
A10
A13
A14
A15
VDD
VSS
PVCC
A5
A4
A3
A1
EN
B7
B6
B9
B8
VM
B3
B4
B5
VINT
Ib_o
Ib−
Ib+
PWM
EN
HOW
LOW
LOV
HOV
VM
HOU
LOU
FGOUT
J1
C6
R35
C12
R30
R14
R8
C5
C19
Ia+
Ia−
Ia_o
I_a
I_p
BRK
VDET
NRST
Data
CLK
DIR
VDC
GND
VSP
FG_OUT
BRK
CON2
R5
TX
D4
C4
R15
C11
R3
R4
C15
R36
C9
D2
R26
R32
R22
R23
R25
C20
C21
5V
DATA
CLK
GND
CON5
D1
b
R33
C10
C7
R7
U
1
U
V
W
3
CON6
3
5V
GND
Hall
1
CON1
inergy
PCB−P−T284 V.03
iU639x QFN28 EVB
60
70

TOP OVERLAY

70
80
BOTTOM OVERLAY